IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

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Abstract: IEEE Std 1241-2000 identifies analog-to-digital converter (ADC) error sources and provides test methods with which to perform the required error measurements. The information in this standard is useful both to manufacturers and to users of ADCs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. In some applications, the information provided by the tests described in this standard can be used to correct ADC errors, e.g., correction for gain and offset errors. This standard also presents terminology and definitions to aid the user in defining and testing ADCs.
Keywords: ADC, A/D converter, analog-to-digital converter, digitizer, terminology, test methods

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Introduction

(This introduction is not a part of IEEE Std 1241-2000, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.)

This standard defines the terms, definitions, and test methods used to specify, characterize, and test analog-to-digital converters (ADCs). It is intended for the following:

— Individuals and organizations who specify ADCs to be purchased

— Individuals and organizations who purchase ADCs to be applied in their products

— Individuals and organizations whose responsibility is to characterize and write reports on ADCs available for use in specific applications

— Suppliers interested in providing high-quality and high-performance ADCs to acquirers

This standard is designed to help organizations and individuals

— Incorporate quality considerations during the definition, evaluation, selection, and acceptance of supplier ADCs for operational use in their equipment

— Determine how supplier ADCs should be evaluated, tested, and accepted for delivery to end users

This standard is intended to satisfy the following objectives:

— Promote consistency within organizations in acquiring third-party ADCs from component suppliers

— Provide useful practices on including quality considerations during acquisition planning

— Provide useful practices on evaluating and qualifying supplier capabilities to meet user requirements

— Provide useful practices on evaluating and qualifying supplier ADCs

— Assist individuals and organizations judging the quality and suitability of supplier ADCs for referral to end users

Several standards have previously been written that address the testing of analog-to-digital converters either directly or indirectly. These include

— IEEE Std 1057-1994[a], which describes the testing of waveform recorders. This standard has been used as a guide for many of the techniques described in this standard.

— IEEE Std 746-1984 [B16][b], which addresses the testing of analog-to-digital and digital-to-analog converters used for PCM television video signal processing.

— JESD99-1 [B21], which deals with the terms and definitions used to describe analog-to-digital and digital-to-analog converters. This standard does not include test methods.

IEEE Std 1241-2000 for analog-to-digital converters is intended to focus specifically on terms and definitions as well as test methods for ADCs for a wide range of applications.

[a]Information on references can be found in Clause 2.
[b]The numbers in brackets correspond to those in the bibliography in Annex C.

As of October 2000, the working group had the following membership:

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W. Thomas Meyer, *Figures Editor*

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Contributions were also made in prior years by:

Jerry Blair	John Deyst	Norris Nahman
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Steve Broadstone	Yves Langard	T. Michael Souders

The following members of the balloting committee voted on this standard:

Pasquale Arpaia	Pasquale Daponte	W. Thomas Meyer
Suresh Babu	Philip Green	Carlo Morandi
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IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

1. Overview

This standard is divided into four clauses plus annexes. Clause 1 is a basic orientation. For further investigation, users of this standard can consult Clause 2, which contains references to other IEEE standards on waveform measurement and relevant International Standardization Organization (ISO) documents. The definitions of technical terms and symbols used in this standard are presented in Clause 3. Clause 4 presents a wide range of tests that measure the performance of an analog-to-digital converter. Annexes, containing the bibliography and informative comments on the tests presented in Clause 4, augment the standard.

1.1 Scope

The material presented in this standard is intended to provide common terminology and test methods for the testing and evaluation of analog-to-digital converters (ADCs). This standard considers only those ADCs whose output values have discrete values at discrete times, i.e., they are quantized and sampled. In general, this quantization is assumed to be nominally uniform (the input–output transfer curve is approximately a straight line) as discussed further in 1.3, and the sampling is assumed to be at a nominally uniform rate. Some but not all of the test methods in this standard can be used for ADCs that are designed for non-uniform quantization.

This standard identifies ADC error sources and provides test methods with which to perform the required error measurements. The information in this standard is useful both to manufacturers and to users of ADCs in that it provides a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. In some applications, the information provided by the tests described in this standard can be used to correct ADC errors, e.g., correction for gain and offset errors.

The reader should note that this standard has many similarities to IEEE Std 1057-1994. Many of the tests and terms are nearly the same, since ADCs are a necessary part of digitizing waveform recorders.

1.2 Analog-to-digital converter background

This standard considers only those ADCs whose output values have discrete values at discrete times, i.e., they are quantized and sampled. Although different methods exist for representing a continuous analog signal as a discrete sequence of binary words, an underlying model implicit in many of the tests in this standard assumes that the relationship between the input signal and the output values approximates the staircase transfer curve depicted in Figure 1a. Applying this model to a voltage-input ADC, the full-scale input range (FS) at the ADC is divided into uniform intervals, known as code bins, with nominal width Q. The number of code transition levels in the discrete transfer function is equal to 2^N-1, where N is the number of digitized bits of the ADC. Note that there are ADCs that are designed such that N is not an integer, i.e., the number of code transition levels is not an integral power of two. Inputs below the first transition or above the last transition are represented by the most negative and positive output codes, respectively. Note, however, that two conventions exist for relating $V_{\min}$ and $V_{\max}$ to the nominal transition points between code levels, *mid-tread* and *mid-riser*.

The dotted lines at $V_{\min}$, $V_{\max}$, and $(V_{\min} + V_{\max})/2$ indicate what is often called the *mid-tread* convention, where the first transition is $Q/2$ above $V_{\min}$ and the last transition is $3Q/2$, below $V_{\max}$. This convention gets its name from the fact that the midpoint of the range, $(V_{\min} + V_{\max})/2$, occurs in the middle of a code, i.e., on the *tread* of the staircase transfer function. The second convention, called the *mid-riser* convention, is indicated in the figure by dashed lines at $V_{\min}$, $V_{\max,}$ and $(V_{\min} + V_{\max})/2$. In this convention, $V_{\min}$ is $-Q$ from the first transition, $V_{\max}$ is $+Q$ from the last transition, and the midpoint, $(V_{\min} + V_{\max})/2$, occurs on a staircase riser. The difference between the two conventions is a displacement along the voltage axis by an amount $Q/2$.

For all tests in this standard, this displacement has no effect on the results and either convention may be used. The one place where it does matter is when a device provides or expects user-provided reference signals. In this case the manufacturer must provide the necessary information relating the reference levels to the code transitions. In both conventions the number of code transitions is 2^N-1 and the full-scale range, FSR, is from $V_{\min}$ to $V_{\max}$. Even in an ideal ADC, the quantization process produces errors. These errors contribute to the difference between the actual transfer curve and the ideal straight-line transfer curve, which is plotted as a function of the input signal in Figure 1b.

To use this standard, the user must understand how the transfer function maps its input values to output codewords, and how these output codewords are converted to the code bin numbering convention used in this standard. As shown in Figure 1a, the lowest code bin is numbered 0, the next is 1, and so on up to the highest code bin, numbered (2^N-1). In addition to unsigned binary (Figure 1a), ADCs may use 2's complement, sign-magnitude, Gray, Binary-Coded-Decimal (BCD), or other output coding schemes. In these cases, a simple mapping of the ADC's consecutive output codes to the unsigned binary codes can be used in applying various tests in this standard. Note that in the case of an ADC whose number of distinct output codes is not an integral power of 2 (e.g., a BCD-coded ADC), the number of digitized bits N is still defined, but will not be an integer.

Real ADCs have other errors in addition to the nominal quantization error shown in Figure 1b. All errors can be divided into the categories of static and dynamic, depending on the rate of change of the input signal at the time of digitization. A slowly varying input can be considered a static signal if its effects are equivalent to those of a constant signal. Static errors, which include the quantization error, usually result from non-ideal spacing of the code transition levels. Dynamic errors occur because of additional sources of error induced by the time variation of the analog signal being sampled. Sources include harmonic distortion from the analog input stages, signal-dependent variations in the time of samples, dynamic effects in internal amplifier and comparator stages, and frequency-dependent variation in the spacing of the quantization levels.

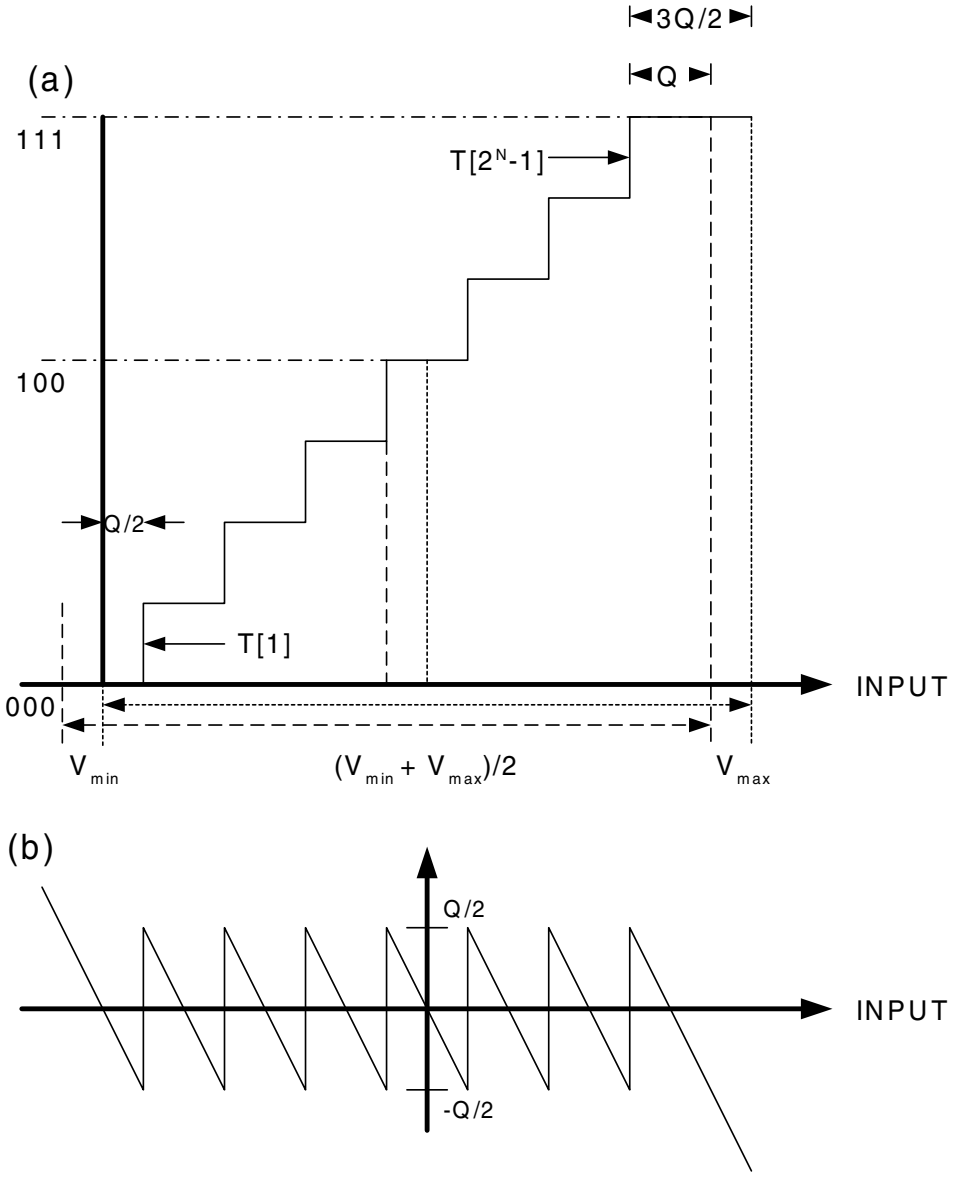

Figure 1—Staircase ADC transfer function, having full-scale range FSR and 2^N-1 levels, corresponding to *N*-bit quantization

1.3 Guidance to the user

1.3.1 Interfacing

ADCs present unique interfacing challenges, and without careful attention users can experience substandard results. As with all mixed-signal devices, ADCs perform as expected only when the analog and digital domains are brought together in a well-controlled fashion. The user should fully understand the manufacturer's recommendations with regard to proper signal buffering and loading, input signal connections, transmission line matching, circuit layout patterns, power supply decoupling, and operating conditions. Edge characteristics for start-convert pulse(s) and clock(s) must be carefully chosen to ensure that input signal purity is maintained with sufficient margin up to the analog input pin(s). Most manufacturers now provide excellent ADC evaluation boards, which demonstrate

recommended layout techniques, signal conditioning, and interfacing for their ADCs. If the characteristics of a new ADC are not well understood, then these boards should be analyzed or used before starting a new layout.

1.3.2 Test conditions

ADC test specifications can be split into two groups: test conditions and test results. Typical examples of the former are: temperature, power supply voltages, clock frequency, and reference voltages. Examples of the latter are: power dissipation, effective number of bits, spurious free dynamic range (SFDR), and integral non-linearity (INL). The test methods defined in this standard describe the measurement of test results for given test conditions.

ADC specification sheets will often give allowed ranges for some test condition (e.g., power supply ranges). This implies that the ADC will function properly and that the test results will fall within their specified ranges for all test conditions within their specified ranges.

Since the test condition ranges are generally specified in continuous intervals, they describe an infinite number of possible test conditions, which obviously cannot be exhaustively tested. It is up to the manufacturer or tester of an ADC to determine from design knowledge and/or testing the effect of the test conditions on the test result, and from there to determine the appropriate set of test conditions needed to accurately characterize the range of test results. For example, knowledge of the design may be sufficient to know that the highest power dissipation (test result) will occur at the highest power supply voltage (test condition), so the power dissipation test need be run only at the high end of the supply voltage range to check that the dissipation is within the maximum of its specified range. It is very important that relevant test conditions be stated when presenting test results.

1.3.3 Test equipment

One must ensure that the performance of the test equipment used for these tests significantly exceeds the desired performance of the ADC under evaluation. Users will likely need to include additional signal conditioning in the form of filters and pulse shapers. Accessories such as terminators, attenuators, delay lines, and other such devices are usually needed to match signal levels and to provide signal isolation to avoid corrupting the input stimuli.

Quality testing requires following established procedures, most notably those specified in ISO 9001: 2000 [B18]. In particular, traceability of instrumental calibration to a known standard is important. Commonly used test setups are described in 4.1.1.

1.3.4 Test selection

When choosing which parameters to measure, one should follow the outline and hints in this clause to develop a procedure that logically and efficiently performs all needed tests on each unique setup. The standard has been designed to facilitate the development of these test procedures. In this standard the discrete Fourier transform (DFT) is used extensively for the extraction of frequency domain parameters because it provides numerous evaluation parameters from a single data record. DFT testing is the most prevalent technique used in the ADC manufacturing community, although the sine-fit test, also described in the standard, provides meaningful data. Nearly every user requires that the ADC should meet or exceed a minimum signal-to-noise-and-distortion ratio (SINAD) limit for the application and that the nonlinearity of the ADC be well understood. Certainly, the extent to which

this standard is applied will depend upon the application; hence, the procedure should be tailored for each unique characterization plan.

1.4 Manufacturer-supplied information

1.4.1 General information

Manufacturers shall supply the following general information:

a) Model number
b) Physical characteristics: dimensions, packaging, pinouts
c) Power requirements
d) Environmental conditions: Safe operating, non-operating, and specified performance temperature range; altitude limitations; humidity limits, operating and storage; vibration tolerance; and compliance with applicable electromagnetic interference specifications
e) Any special or peculiar characteristics
f) Compliance with other specifications
g) Calibration interval, if required by ISO 10012-2:1997 [B19]
h) Control signal characteristics
i) Output signal characteristics
j) Pipeline delay (if any)
k) Exceptions to the above parameters where applicable

1.4.2 Minimum specifications

The manufacturer shall provide the following specifications (see Clause 3 for definitions):

a) Number of digitized bits
b) Range of allowable sample rates
c) Analog bandwidth
d) Input signal full-scale range with nominal reference signal levels
e) Input impedance
f) Reference signal levels to be applied
g) Supply voltages
h) Supply currents (max, typ)
i) Power dissipation (max, typ)

1.4.3 Additional specifications

a) Gain error
b) Offset error
c) Differential nonlinearity
d) Harmonic distortion and spurious response
e) Integral nonlinearity
f) Maximum static error
g) Signal-to-noise ratio
h) Effective bits
i) Random noise
j) Frequency response

k) Settling time
l) Transition duration of step response (rise time)
m) Slew rate limit
n) Overshoot and precursors
o) Aperture uncertainty (short-term time-base instability)
p) Crosstalk
q) Monotonicity
r) Hysteresis
s) Out-of-range recovery
t) Word error rate
u) Common-mode rejection ratio
v) Maximum common-mode signal level
w) Differential input impedance
x) Intermodulation distortion
y) Noise power ratio
z) Differential gain and phase

1.4.4 Critical ADC parameters

Table 1 is presented as a guide for many of the most common ADC applications. The wide range of ADC applications makes a comprehensive listing impossible. This table is intended to be a helpful starting point for users to apply this standard to their particular applications.

Table 1—Critical ADC parameters

Typical applications	Critical ADC parameters	Performance issues
Audio	SINAD, THD	Power consumption. Crosstalk and gain matching.
Automatic control	Monotonicity Short-term settling, long-term stability	Transfer function. Crosstalk and gain matching. Temperature stability.
Digital oscilloscope/waveform recorder	SINAD, ENOB Bandwidth Out-of-range recovery Word error rate	SINAD for wide bandwidth amplitude resolution. Low thermal noise for repeatability. Bit error rate.
Geophysical	THD, SINAD, long-term stability	Millihertz response.
Image processing	DNL, INL, SINAD, ENOB Out-of-range recovery Full-scale step response	DNL for sharp-edge detection. High-resolution at switching rate. Recovery for blooming.
Radar and sonar	SINAD, IMD, ENOB SFDR Out-of-range recovery	SINAD and IMD for clutter cancellation and Doppler processing.
Spectrum analysis	SINAD, ENOB SFDR	SINAD and SFDR for high linear dynamic range measurements.
Spread spectrum communication	SINAD, IMD, ENOB SFDR, NPR Noise-to-distortion ratio	IMD for quantization of small signals in a strong interference environment. SFDR for spatial filtering. NPR for interchannel crosstalk.
Telecommunication personal communications	SINAD, NPR, SFDR, IMD Bit error rate Word error rate	Wide input bandwidth channel bank. Interchannel crosstalk. Compression. Power consumption.

Table 1—Critical ADC parameters *(continued)*

Typical applications	Critical ADC parameters	Performance issues
Video	DNL, SINAD, SFDR, DG, DP	Differential gain and phase errors. Frequency response.
Wideband digital receivers SIGINT, ELINT, COMINT	SFDR, IMD SINAD	Linear dynamic range for detection of low-level signals in a strong interference environment. Sampling frequency.

COMINT = communications intelligence
DNL = differential nonlinearity
ENOB = effective number of bits
ELINT = electronic intelligence
NPR = noise power ratio
INL = integral nonlinearity
DG = differential gain error
SIGINT = signal intelligence
SINAD = signal-to-noise and distortion ratio
THD = total harmonic distortion
IMD = intermodulation distortion
SFDR = spurious free dynamic range
DP = differential phase error

2. References

This standard shall be used in conjunction with the following publications. When the following specifications are superseded by an approved revision, the revision shall apply.

IEC 60469-2 (1987-12), Pulse measurement and analysis, general considerations.[1]

IEEE Std 1057-1994, IEEE Standard for Digitizing Waveform Recorders.[2]

3. Definitions and symbols

For the purposes of this standard, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standards Terms* [B15] should be referenced for terms not defined in this clause.

3.1 Definitions

3.1.1 AC-coupled analog-to-digital converter: An analog-to-digital converter utilizing a network which passes only the varying ac portion, not the static dc portion, of the analog input signal to the quantizer.

3.1.2 alternation band: The range of input levels which causes the converter output to alternate between two adjacent codes. A property of some analog-to-digital converters, it is the complement of the hysteresis property.

3.1.3 analog-to-digital converter (ADC): A device that converts a continuous time signal into a discrete-time discrete-amplitude signal.

3.1.4 aperture delay: The delay from a threshold crossing of the analog-to-digital converter clock which causes a sample of the analog input to be taken to the center of the aperture for that sample.

[1]IEC publications are available from IEC Sales Department, Case Postale 131, 3 rue de Varemb, CH 1211, Gen ve 20, Switzerland/Suisse (http://www.iec.ch). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 25 W. 43rd Street, Fourth Floor, New York, NY 10036, USA (http://www.ansi.org).
[2]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://standards.ieee.org/).

3.1.5 aperture jitter: *See:* **aperture uncertainty.**

3.1.6 aperture uncertainty: The standard deviation of the sample instant in time. *Syn:* **aperture jitter, timing jitter, timing phase noise.**

3.1.7 asynchronous sampling: Refers to sampling an input signal that is not phase locked to the analog-to-digital converter sampling frequency.

3.1.8 clock signal duty cycle: The fraction of the time the clock signal spends in excess of the logic threshold.

3.1.9 clock signal slew rate: The time derivative of the clock signal at the point where it crosses the logic threshold.

3.1.10 code bin (k): A digital output that corresponds to a particular set of input values.

3.1.11 code bin width ($W[k]$): The difference of the code transition levels, $T[k+1]$ and $T[k]$, that delimit the kth bin:

$$W[k] = T[k+1] - T[k] \tag{1}$$

3.1.12 code transition level: The boundary between two adjacent code bins.

3.1.13 code transition level ($T[k]$): The value of the converter-input parameter at the transition point between two given adjacent code bins. The transition point is defined as the input value that causes 50% of the output codes to be greater than or equal to the upper code of the transition, and 50% to be less than the upper code of the transition. The transition level $T[k]$ lies between code bin $k-1$ and code bin k.

3.1.14 coherent sampling: Sampling of a periodic waveform such that there is an integer number of waveform cycles in the data record. Coherent sampling occurs when the following relationship exists:

$$f_s \times J = f_r \times M \tag{2}$$

where

f_s is the sampling frequency,

J is the integer number of cycles of the waveform in the data record,

f_r is the reciprocal of the period of the waveform,

M is the number of samples in the data record.

3.1.15 common-mode out-of-range: A signal level whose magnitude is less than the specified maximum safe common-mode signal but greater than the maximum operating common-mode signal.

3.1.16 common-mode out-of-range recovery time: The time required for the analog-to-digital converter under test to return to its specified characteristics after the end of a common-mode out-of-range input signal.

3.1.17 common-mode range: The range of analog input signal swing at each differential input over which the common-mode rejection is specified. Common-mode range is also the sum of the largest simultaneously applied common-mode signal and differential signal.

3.1.18 common-mode rejection ratio (CMRR): The ratio of the input common-mode signal to the effect produced at the output of the analog-to-digital converter under test, in units of the input signal.

3.1.19 common-mode signal: The average value of the signals at the positive input and the negative input of a differential-input analog-to-digital converter. If the signal at the positive input is designated V_+, and the signal at the negative input is designated V_-, then the common-mode signal V_{cm} is

$$V_{\text{cm}} = \frac{V_+ + V_-}{2} \tag{3}$$

3.1.20 conversion (clock) rate (f_s): The frequency at which digital output words are provided by the analog-to-digital converter on its output.

3.1.21 crosstalk: Undesired energy appearing in a signal as a result of coupling from other signals.

3.1.22 data valid time: A measure of the time, in analog-to-digital converter clock cycles, between the first clock transition after the data becomes valid at the digital outputs and the last clock transition before it becomes invalid.

3.1.23 differential-input impedance to ground: For a differential-input analog-to-digital converter, the impedance between the positive input and the negative input.

3.1.24 differential nonlinearity (DNL): The difference between a specified code bin width and the average code bin width, divided by the average code bin width.

3.1.25 differential signal: The difference between the signal at the positive and negative inputs of a differential-input analog-to-digital converter. If the signal at the positive input is designated V_+, and the signal at the negative input is designated V_-, then the differential signal (V_{dm}) is

$$V_{\text{dm}} = V_+ - V_- \tag{4}$$

3.1.26 effective number of bits (ENOB): A measure of the signal-to-noise and distortion ratio used to compare actual analog-to-digital converter (ADC) performance to an ideal ADC.

3.1.27 epoch: The duration of time corresponding to a data record. For instance, for an M-sample record acquired at the uniform sampling period T_s, the epoch is MT_s.

3.1.28 equivalent-time sampling: A process by which consecutive samples of a repetitive waveform are acquired and assembled from multiple repetitions of the waveform, to produce a record of samples representing a single repetition of the waveform.

3.1.29 fall time (t_F): The time for the desired signal to go from 90% to 10% of the transition range.

3.1.30 full-scale range (FSR): The difference between the most positive and most negative analog inputs of a converter's operating range. For an N-bit converter, FSR is given by:

$$\text{FSR} = (2^N)(\text{ideal code width}) \tag{5}$$

in analog input units.

3.1.31 full-scale signal: A full-scale signal is one whose peak-to-peak amplitude spans the entire range of input values recordable by the analog-to-digital converter under test.

3.1.32 full-width-at-half-max (FWHM): The width of a distribution measured at an amplitude of one half of the maximum amplitude.

3.1.33 gain and offset: (A) (independently based) Gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to minimize the mean squared deviation from the output values. **(B) (terminal-based)** Gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to cause the deviations from the output values to be zero at the terminal points, that is, at the first and last codes.

3.1.34 harmonic distortion: For a pure sine wave input, output components at frequencies that are an integer multiple of the applied sine wave frequency which are induced by the input sine wave.

3.1.35 hysteresis: The maximum difference in values of a code transition level, when the transition level is approached by a changing input signal from either side of the transition.

3.1.36 ideal code bin width (Q): The ideal full-scale input range divided by the total number of code bins.

3.1.37 incoherent sampling: Sampling of a waveform such that the relationship between the input frequency, sampling frequency, number of cycles in the data record, and the number of samples in the data record does not meet the definition of coherent sampling.

3.1.38 input impedance: The impedance between the signal input of the analog-to-digital converter under test and ground.

3.1.39 integral nonlinearity (INL): The maximum difference between the ideal and actual code transition levels after correcting for gain and offset.

3.1.40 kth code transition level ($T[k]$): The input value corresponding to the transition between codes $k-1$ and k. (See Figure 2.)

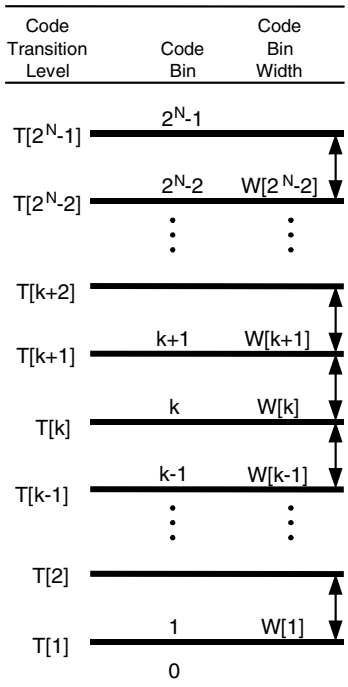

Figure 2—Definitions pertaining to input quantization

3.1.41 large signal: One whose peak-to-peak amplitude is as large as practical but is recorded by the instrument within, but not including, the maximum and minimum amplitude data codes. As a minimum, the signal must span at least 90% of the full-scale range of the analog-to-digital converter under test.

3.1.42 least significant bit (LSB): With reference to analog-to-digital converter input signal amplitude, is synonymous with one ideal code bin width.

3.1.43 logic level: Any level within one of two (or more) non-overlapping ranges of values, of a physical quantity, used to represent the logic states (IEEE 100 [B15]).

3.1.44 long-term settling error: The absolute difference between the final value specified for short-term settling time and the value 1 s after the beginning of the step, expressed as a percentage of the step amplitude.

3.1.45 maximum common-mode signal level: The maximum level of the common-mode signal at which the common-mode rejection ratio is still valid.

3.1.46 maximum operating common-mode signal: The largest common-mode signal for which the analog-to-digital converter will meet its specifications when recording a simultaneously applied, normal-mode signal.

3.1.47 maximum safe input signal level: The input level beyond which damage to the device may occur.

3.1.48 monotonic analog-to-digital converter: An analog-to-digital converter that has output codes that do not decrease (increase) for a uniformly increasing (decreasing) input signal, disregarding random noise.

3.1.49 noise power ratio: The ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the discrete Fourier transform spectrum of the analog-to-digital converter output sample set.

3.1.50 noise (total): Any deviation between the output signal (converted to input units) and the input signal except deviations caused by linear time-invariant system response (gain and phase shift), or a dc level shift. For example, noise includes the effects of random errors (random noise), fixed pattern errors, nonlinearities (e.g., harmonic or intermodulation distortion), and aperture uncertainty. *See also*: **random noise**.

3.1.51 normal mode signal: The difference between the signal at the positive input and the negative input of a differential input analog-to-digital converter. *Syn:* differential signal.

3.1.52 offset: *See:* **gain and offset**.

3.1.53 out-of-range input: Any input whose magnitude is less than the maximum safe input signal of the analog-to-digital converter but greater than the full-scale range.

3.1.54 overshoot: The maximum amount by which the step response exceeds the topline, specified as a percentage of (recorded) pulse amplitude.

3.1.55 passband: The band of input signal frequencies that the analog-to-digital converter is intended to digitize with nominally constant gain.

3.1.56 phase nonlinearity: The deviation in phase response from a perfectly linear-phase response as a function of frequency.

3.1.57 pipeline delay: A measure of the latency in terms of analog-to-digital converter clock cycles between the clock transition that initiates sampling of the input and the presentation of the digitized value of that sample at the digital output.

3.1.58 precursor: In a step or pulse waveform, any deviation from the baseline prior to the pulse transition.

3.1.59 probability density function (PDF): For a random variable, x, a positive real monotonic non-decreasing function, $f_x(x)$, which has the interpretation that $f_x(x)\,\mathrm{d}x$ is the probability that the random variable, X, lies in the interval $(x, x+\mathrm{d}x)$.

3.1.60 quantization: A process in which the continuous range of values of an input signal is divided into non-overlapping sub-ranges, and to each sub-range a discrete value of the output is uniquely assigned. Whenever the signal value falls within a given sub-range, the output has the corresponding discrete value. (See IEEE 100 [B15].)

3.1.61 quantization error/quantization noise: The error caused by conversion of a variable having a continuous range of values to a quantized form having only discrete values, as in analog-to-digital conversion. The error is the difference between the original (analog) value and its quantized (digital) representation. (See IEEE 100 [B15].)

3.1.62 random noise: A non-deterministic fluctuation in the output of an analog-to-digital converter, described by its frequency spectrum and its amplitude statistical properties. *See also:* **noise**.

3.1.63 record of data: A sequential collection of samples acquired by the analog-to-digital converter.

3.1.64 relatively prime: Describes integers whose greatest common divisor is 1.

3.1.65 residuals: In curve fitting, the differences between the recorded data and the fitted function.

3.1.66 rise time (t_R): The time for the signal to go from 10% to 90% of the transition range.

3.1.67 root-mean-square (rms): For a given set of data, the square root of the arithmetic mean of the squared values of each of the data.

3.1.68 root-sum-square (rss): For a given set of data, the square root of the sum of the squared values of each of the data.

3.1.69 sampling: The process of assigning discrete time values to a continuous time signal.

3.1.70 settling time: The time at which the step response enters and subsequently remains within a specified error band around the final value, measured from the mesial point (50%) of the response. The final value is defined to occur 1 s after the beginning of the step.

3.1.71 short-term settling time: Measured from the mesial point (50%) of the output, the time at which the **step response** enters and subsequently remains within a specified error band around the final value. The final value is defined to occur at a specified time less than 1 s after the beginning of the step.

3.1.72 signal-to-noise and distortion ratio (SINAD): For a pure sine wave input of specified amplitude and frequency, the ratio of the root-mean-square (rms) amplitude of the analog-to-digital converter output signal to the rms amplitude of the output noise, where noise is defined as above to include not only random errors but also nonlinear distortion and the effects of sampling time errors.

NOTE—Signal-to-noise and distortion ratio in this standard is equivalent to signal-to-noise-ratio in IEEE Std 1057-1994.

3.1.73 single-ended analog-to-digital converter: A non-differential analog-to-digital converter, i.e., one that does not subtract the signals at two input terminals. Such a converter may add multiple inputs.

3.1.74 slew limit: The value of output transition rate of change for which an increased amplitude input step signal causes no change.

3.1.75 small signal: A signal whose peak-to-peak amplitude spans no more than 10% of the full range of the analog-to-digital converter under test.

3.1.76 Signal to non-harmonic ratio (SNHR): For a pure sine-wave input of specified amplitude and frequency, the ratio of the root-mean-square (rms) amplitude of the analog-to-digital converter output signal to the rms amplitude of the output noise which is not harmonic distortion.

3.1.77 SNR: Typically, this refers to "signal-to-noise" ratio. In the context of analog-to-digital converters, the term SNR is ambiguous, since it has been used to represent both signal-to-noise and distortion ratio (SINAD) and signal to non-harmonic ratio (SNHR); therefore, we will not use it in this standard.

3.1.78 spurious components: Persistent sine waves at frequencies other than the harmonic frequencies. *See:* **harmonic distortion.**

3.1.79 spurious-free dynamic range (SFDR): For a pure sinewave input of specified amplitude and frequency, the ratio of the amplitude of the analog-to-digital converter's output averaged spectral component at the input frequency, f_i, to the amplitude of the largest harmonic or spurious spectral component observed over the full Nyquist band, $\max\{|X(f_h)| \text{ or } |X(f_s)|\}$:

$$\mathrm{SFDR(dB)} = 20\log_{10}(|X_{avg}(f_i)|/\max_{f_s, f_h}\{|X_{avg}(f_h)| \text{ or } |X_{avg}(f_s)|\}) \tag{6}$$

where

X_{avg} is the averaged spectrum of the ADC output,

f_r is the input signal frequency,

f_h and f_s are the frequencies of the set of harmonic and spurious spectral components.

3.1.80 step (or pulse) baseline: The magnitude reference line at the base magnitude [IEC 60649-2 (1987-12)].

3.1.81 step (or pulse) topline: The magnitude reference line at the top magnitude [IEC 60649-2 (1987-12)].

3.1.82 step response: The recorded output response for an ideal input step with designated baseline and topline.

3.1.83 synchronous sampling: Refers to sampling an input signal that has been phase locked to the analog-to-digital converter sampling frequency.

3.1.84 timing jitter: *See:* **aperture uncertainty.**

3.1.85 timing phase noise: *See:* **aperture uncertainty.**

3.1.86 total harmonic distortion (THD): For a pure sinewave input of specified amplitude and frequency, the root-sum-of-squares (rss) of all the harmonic distortion components including their aliases in the spectral output of the analog-to-digital converter. Unless otherwise specified, THD is estimated by the rss of the second through the tenth harmonics, inclusive. THD is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency.

3.1.87 total spurious distortion (TSD): For a pure sinewave input of specified amplitude and frequency, the root-sum-square of the spurious components in the spectral output of the analog-to-digital converter. TSD is often expressed as a decibel ratio with respect to the root-mean-square amplitude of the output component at the input frequency.

3.1.88 transfer curve: The representation of the average digital output code of an analog-to-digital converter as a function of the input signal value.

3.1.89 transition duration of a step response: The duration between the 10% point and the 90% point on the recorded step response transition, for an ideal input step with designated baseline and topline.

3.1.90 useful power bandwidth: The large signal analog input frequency at which a record of the analog-to-digital converter's output data will be degraded by less than a specified amount.

3.1.91 voltage standing wave ratio (VSWR): The ratio of the mismatch between the actual impedance and the desired or nominal impedance.

3.1.92 window: A set of coefficients with which corresponding samples in a data record are multiplied so as to more accurately estimate certain properties of the signal, particularly frequency domain properties. Generally the coefficient values increase smoothly toward the center of the record.

3.1.93 word error rate: The probability of receiving an erroneous code for an input after correction is made for gain, offset, and linearity errors, and a specified allowance is made for random noise. Typical causes of word errors are metastability and timing jitter of comparators within the analog-to-digital converter.

3.2 Symbols and acronyms

ε error, used for total error and error band

ε_{rms} root-mean-square value of ε

$\varepsilon[k]$ difference between $T[k]$ and ideal value of $T[k]$ computed from G and V_{os}

θ phase, expressed as radians

π ratio of the circumference of a circle to the diameter (constant)

ρ reflection coefficient

σ standard deviation; sometimes used as noise amplitude, which is the standard deviation of the random component of a signal

σ_σ standard deviation of the standard deviation (e.g., standard deviation of the noise amplitude)

σ_t aperture uncertainty

σ^2 variance; sometimes used to describe random noise power

τ sampling period, the inverse of f_s

ω $2\pi f =$ angular frequency, expressed in radians per second

ω_i	angular input frequency expressed in radians per second
a	general purpose real number
A	sinusoidal amplitude
B	test tolerance in fractions of a least significant bit (Q); also used as an amplitude
C	offset
CMR	common-mode range
D	general purpose integer
DNL	maximum differential nonlinearity over all k $d[n]$ = dither component of output sample $y[n]$
DNL[k]	differential nonlinearity of code k
d_{est} [n]	estimate of the dither component $d[n]$
E_{G} (f)	gain flatness error of frequency f
ENBW	equivalent noise bandwidth
ENOB	effective number of bits
$e_{\text{m}}[f]$	aliasing and first differencing magnitude errors
$e_{\text{p}}[f]$	aliasing and first differencing phase errors
FSR	full-scale range
f	frequency
$f(n)$	sinewave component of output sample $y(n)$
f_{co}	upper frequency for which the amplitude response is −3 dB
f_{d}	sampling frequency of a record after decimation by an integer
f_{eq}	equivalent sampling rate
f_h	frequency of a harmonic of the input frequency
f_{i}	actual input frequency or approximate desired input frequency
f_{imf}	frequency of intermodulation distortion products
f_m	frequency of the mth component of a magnitude spectrum produced by a DFT
f_{opt}	optimum input frequency for testing
f_{r}	input signal reference frequency or input signal repetition rate

f_s	sampling frequency
f_{sp}	frequency of a persistent spurious tone
G	static gain of the ADC under test
$G(f)$	dynamic gain of the ADC under test, as a function of frequency f
H	average number of histogram samples received in two code bins sharing the same transition level
$H(f)$	frequency response of the ADC under test, as a function of frequency f
$H(f_k)$	DFT of $h(n)$
$H(i)$	number of histogram samples in bin i
$H_c(j)$	number in the jth bin of the cumulative histogram of samples
$h(n)$	discrete time impulse response of a system
INL	integral nonlinearity
INL(k)	integral nonlinearity at output code k
i	general purpose index
J	number of cycles in a record
k	code bin
L	general purpose integer
l	general purpose factor
M	number of sequential samples in a record
$M_+(x)$, $M_-(x)$	number of measurements of the output value at the input value x for increasing and decreasing inputs respectively
M_D	number of samples in one period of pseudorandom dither
M_d	number of samples in a record after decimation
mse	mean square error
N	number of digitized bits. (Note that for certain ADCs, N may not be an integer value.)
NPR	noise power ratio
n	sample index within a record
p	probability
Q	ideal code bin width, expressed in input units

R	error parameter; also used as minimum number of records required
r	general purpose integer
S	set of samples collected over more than one record, also used as an error parameter or as total number of samples used in a histogram
$T[k]$	code transition level between code $k-1$ and code k
THD	estimate of total harmonic distortion
t_{eq}	average equivalent time sampling period
t_f	top to base transition time; fall time
t_n	discrete sample times
t_r	base to top transition time; rise time
t_{wc}	the center point of the aperture time associated with an output sample
u	confidence level expressed as a fraction
V_{cm}	common-mode signal
V_{dm}	differential mode signal
V_o	input signal overdrive; the amount by which an input signal exceeds the ADC full-scale range
V_{os}	input offset of ADC, ideally = 0
VSWR	voltage standing wave ratio
$W[k]$	code bin width of code bin k
w	estimated word error rate
w'	worst-case word error rate
$w(n)$	window function coefficient (for a DFT)
X	number of standard deviations of a Gaussian distribution
$X_{avm}(f_m)$	the averaged magnitude spectral component at discrete frequency f_m after a DFT
x	ADC input signal value; or number of errors detected
$Y[k]$	the M-point discrete Fourier transform of the M-sample record $y[n]$
$y[n] = y_n$	the nth output data sample within a record
$y[n]$	average of y_n over M samples
$y_{n'}$	best fit points to a data record

Z_0 transmission line impedance

Z_t ADC input impedance

$Z_{u/2}$ number of standard deviations that encompass 100 $(1-u)$ % of a Gaussian distribution about the center

4. Test methods

4.1 General

It is assumed that the user/manufacturer has defined safe operating limits for the device under test. These limits are categorized as *absolute* (the limit beyond which the device will be destroyed) and *operating* (the limit beyond which the device will not operate properly). These limits will vary from device to device, depending on the design. It is not the intention of this document to describe the method of setting these limits, only to verify the operation within them. All test procedures described herein apply only to parameters of a device that is operated within its specified limits.

The type of circuitry used to capture the digital data samples produced by the ADC is determined largely by the data rate. Slower ADCs may be interfaced directly to the computer. ADCs often require a buffer memory to acquire data at the ADC sample rate and then download accumulated samples to the computer at a slower rate. Even faster ADCs may require latches and/or de-multiplexers between the ADC and the buffer memory, and perhaps data decimation, as described in 4.1.2.1. A logic analyzer might be used as a buffer memory to capture data for some tests.

4.1.1 Test setup

A few general test setups can be used to perform most of the ADC tests presented in this standard. Test setups that use sine waves, arbitrary waveforms, and pulses are described in the following subclauses. Some tests, such as those for VSWR and out-of-range signals, require setups other than those discussed in the following subclauses.

4.1.1.1 Sine wave test setup

Figure 3 shows the sine wave test setup. Sine waves are commonly used in ADC testing because appropriate sine wave sources are readily available and because it is relatively easy to establish the quality of the sine wave (e.g., with a spectrum analyzer). A sine wave generator provides the test signal while a clock generator provides the clock (or conversion) signal. Also, combining the output of two (or three) sine wave generators can produce two-tone (or three-tone) test signals for intermodulation distortion testing. Additionally, a noise generator's output can be combined with a signal to provide low-level dither (Gray and Stockham [B11]).

If frequency synthesizers are used to generate the test and clock signals, the synthesizers can often be phase-locked to maintain precise phase relationships between the signal and the sampling clock. Phase-locking of synthesizers facilitates testing and simplifies subsequent digital signal processing, by preventing clock/signal walkthrough (beat patterns) that may artificially increase or reduce measured spurious output.

Both the clock and the test signals must be suitable for the test being performed. Filters may be required in either the clock or signal paths to reduce noise or harmonic distortion. For example,

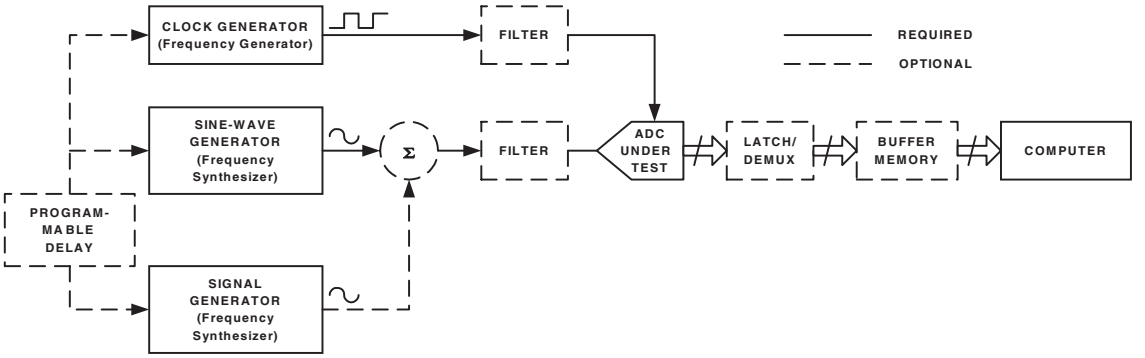

Figure 3—Setup for sine wave testing

sub-harmonics in the clock path will degrade ADC performance, so the clock signal may require filtering to smooth edges which might otherwise feed through to the signal path. Also, low-pass or band-pass filters may be required in the signal path to eliminate noise or other undesirable signals (e.g., harmonics). The relative jitter between the clock and test signals must be low enough to prevent jitter artifacts from affecting the measured noise floor as described in 4.5.2.5.

4.1.1.2 Arbitrary signal test setup

The arbitrary waveform test setup of Figure 4 can be used for arbitrary test signals, such as ramps, chirps, and steps. In this setup, the test signal is generated digitally and then converted to analog. Care must be taken to quantify the performance of the digital-to-analog converter (DAC) and filter in order to assess (or remove) its impact on the measured performance of the ADC under test. See 4.1.1.1 for comments on filters and data capture. It may be suitable to use an arbitrary waveform generator for the DAC and filter functions for some ADCs.

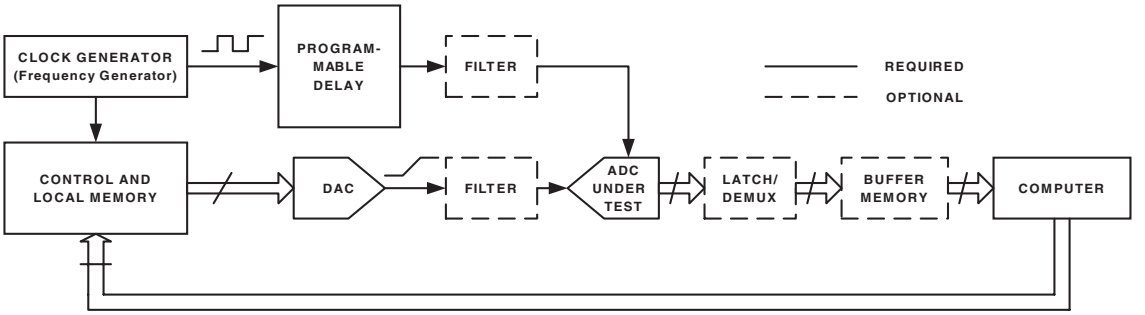

Figure 4—Setup for arbitrary signal testing

4.1.1.3 Step signal setup

Figure 5 shows a step waveform test setup to be used for testing with precision step signals that are not digitally generated. Precision pulses and step signals can be used to measure both time domain parameters (such as impulse response, transition duration, overshoot, and settling time) and frequency domain parameters (such as frequency response amplitude and phase, bandwidth, and gain flatness). Equivalent time sampling can be employed, and certain data analysis tasks can be simplified, if the optional step repetition generator is phase locked to the sampling clock. See 4.1.1.1 for comments on data capture and on filters. Careful attention must be paid to the phase linearity of any filters placed in the pulse/step signal path.

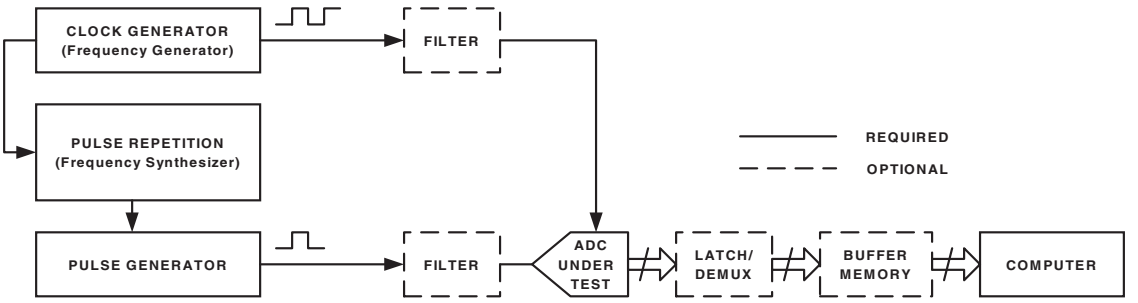

Figure 5—Setup for pulse and step signal testing

4.1.2 Taking a record of data

A record of data is a sequential series of samples acquired by test equipment interfaced to the ADC. The action of taking a record of data is defined as accumulating a set of samples from the ADC using the interfaced test equipment and transferring the sample set to a computer for analysis.

4.1.2.1 Use of output decimation in taking a record of data

For ADCs with very high sample rate, the limits of interfaced memory may make it impractical and/or uneconomical to store sequential samples from the ADC. In this case, output decimation may be used to take a record of data at a slower effective sample rate while still clocking the ADC at the high sample rate. A decimated record is a collection of every Dth sequential sample acquired by the ADC. To do this, a divide-by-D counter is driven by the (high-frequency) ADC clock, and the output of the divider in turn drives a bank of data latches (flip-flops), or triggers a logic analyzer to sample the data outputs of the ADC and pass every Dth sample along to the memory system.

Output decimation may also be applied on tests that do not directly record the output data, for instance when recording histograms of output code occurrences or feeding back the output code to control the input signal level (see 4.1.6.1 and 4.1.6.2). The user should note that decimation involves a loss of information, which in special cases, such as hysteresis testing (see 4.4.4), may affect test results. When output decimation is used, the decimated sample rate, f_s/D, should be used for any equations relating sample rate to input frequency (e.g., for equivalent time sampling) or time measurements (e.g., step response parameters), but the actual ADC sample rate f_s should be quoted as the sample rate in the test results.

For decimation of the output of an ADC system that has a time-interleaved architecture (i.e., L ADCs each sampling at f_s/L), the output decimation ratio D should be made relatively prime to the interleave ratio L; otherwise, the decimated output data stream will not contain data from all of the L interleaved converters.

4.1.3 Equivalent time sampling

The maximum sampling rate of a converter limits its useful measurement bandwidth. Furthermore, if the sampling rate is not at least twice the frequency of the highest frequency component of the input signal, then aliasing errors can result. If the input signal is repetitive, equivalent-time sampling can reduce these limitations. Equivalent-time sampling is a process by which consecutive samples of a repetitive waveform are acquired and assembled from multiple repetitions of the waveform, to produce a record of samples representing a single repetition of the waveform.

Several methods of equivalent-time sampling exist:

a) Apply a known delay between the input signal and the converter's time base

b) Independently measure the relative delay between the signal and the (time base) sample commands

c) Extract equivalent time samples from a single record using the converter's internal time base, provided that the input signal's repetition rate is selected appropriately

The method in 4.1.3.1 implements the extraction method.

4.1.3.1 Extraction method

The method below shows how to use equivalent-time sampling to increase the effective sampling rate by an integer factor D. By appropriate choice of the repetition rate of the input signal (f_i), D periods of the input waveform are recorded in a single record; then, upon rearranging the samples with a simple algorithm, a single period of the input signal is obtained which is effectively sampled at D times the real-time sampling rate. This is illustrated in Figure 6 for $D = 4$. To implement this method, choose integer D based on the required equivalent sample rate, f_{eq}, such that $f_{eq} = Df_s$, where f_s is the ADC sampling frequency. Next, L, the number of real-time samples taken during each repetition of the input waveform, is given by $L = \mathrm{INT}(M/D)$, i.e., the integer value of M/D, where M is the number of samples in a record. Finally, the input signals repetition rate, f_i, is set [as shown in Equation (7)] such that

$$f_i = f_s \frac{D}{LD - 1}, \qquad \text{with } LD \leq M \tag{7}$$

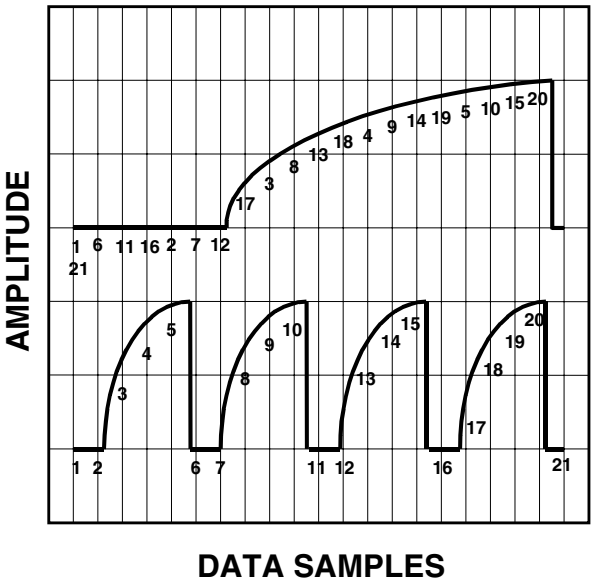

Figure 6—Equivalent time sampling extraction

For the example in Figure 6, $D = 4$, $L = 5$, M could be 20, 21, 22, or 23, and $f_r = 4f_s/19$. (Note that data points between LD and M are not useable). The following pseudo-code implements the algorithm to rearrange the samples in equivalent time:

```
LET F = 0
FOR I = 1 TO L
   FOR J = 1 TO D
      F = F + 1
      I2 = I + (J−1) * L
      E(F) = R(I2)
   NEXT J
NEXT I
```

where

D is the sample rate multiplier,

M is the record length,

L is the INT(M/D) where INT(*) designates the integer part of *,

E(*) is the array containing (L·D) equivalent-time samples,

F is the equivalent-time sampling index,

R(*) is the array containing real-time samples,

I2 is the real-time sampling index.

4.1.3.2 Comments on the extraction method for equivalent time sampling

This method of achieving higher equivalent sampling rates requires that the repetition rate, f_i, of the input signal be precisely controlled. While the average equivalent-time sample rate is just Df_s, independent of f_i, the relative spacing of the equivalent-time samples becomes non-uniform when f_i deviates from the value given by Equation (7). If f_i is too great, $D-1$ out of D successive samples will occur too late while one sample will be correctly placed; if f_i is too small, $D-1$ samples will occur too soon. In either case, the maximum sampling time error (Δt_{eq}) is given, to a good approximation, by Equation (8).

$$\Delta t_{eq} \approx \frac{M(D-1)}{Df_s}\frac{\Delta t_i}{t_i} \tag{8}$$

where

t_{eq} is the average equivalent-time sampling period, i.e., $1/(D \cdot f_s)$,

Δt_{eq} is the maximum sampling time offset,

$\Delta t_i/t_i$ is the proportional error in the repetition period (or repetition rate).

Note, however, that the errors are not cumulative; the average equivalent-time sampling period is still given by $1/Df_s$.

Of course, the assumption is made in Equation (7) that f_s is exactly known; if it is not exactly known, then the additional error given by an expression similar to Equation (8) will accrue. As an example,

if $D = 4$, $M = 1024$, and the equivalent sampling period is known to 5%, then the repetition rate must be set, and the sampling rate must be known, each with an accuracy of $0.05/(1024 \times 3) = 16$ PPM.

To achieve such accuracy it is usually necessary to use a frequency-synthesized source. It may sometimes be necessary to measure the frequency of the input signal as well as the frequency of the ADC's clock generator with an accurate frequency counter to assure that they are set with sufficient accuracy. If sufficient accuracy cannot be guaranteed for a specific record length, the accuracy might be improved by decreasing the record length. However, since the lowest frequency component that is represented in a record of length M is given by f_{eq}/M, this limits the range of frequencies that can be represented.

4.1.3.3 Alternate extraction method

This alternate method of extracting an equivalent time record is based upon a simple keep-one-of-each-D samples decimation of an input record. While the decimation operation could be performed in either hardware or software, the method as outlined here implicitly assumes that the decimation is done in software.

At a sampling frequency, f_s, it is possible to adjust the input frequency, f_i, of a repetitive waveform to obtain exactly one cycle in a record of length M, as shown in Equation (9).

$$f_i = nf_s + \frac{f_s}{M} \qquad n = 0, 1, 2, 3 \ldots \tag{9}$$

Intentional aliasing of the input occurs when n is greater than or equal to one. The usual concern about not being able to tell which alias is observed does not apply in the practical case, as the input signal is known a priori.

When an ADC output data record is decimated by the factor D, the decimated output is sampled at a sampling frequency f_d; when a record of length M is decimated by keeping only one of every D samples it will be of length M_d, as shown in Equation (10) and Equation (11).

$$f_d = \frac{f_s}{D} \tag{10}$$

$$M_d = \frac{M}{D} \tag{11}$$

When f_d is substituted for f_s and M_d for M in Equation (9), and using the relation $f_d/M_d = f_s/M$, then one cycle in a record of length M_d results from the input frequency chosen using Equation (12).

$$f_i = nf_d + \frac{f_s}{M} \qquad n = 0, 1, 2, 3 \ldots \tag{12}$$

When a decimated record of length M_d contains a single cycle of f_i, the equivalent sampling rate, f_{eq}, is the number of points in the decimated record divided by the period of the single cycle. Thus f_{eq} is equivalent to the frequency f_i times the length M_d, as shown in Equation (13).

$$f_{eq} = f_i M_d \tag{13}$$

This method uses input frequencies determined by Equation (12) with n chosen to be an appropriate integer in order to yield an equivalent time record of M_d samples at various frequencies of interest. The resulting records contain a single cycle in a record of length M_d. Each increment of n yields a proportional increase in f_{eq}. If fast Fourier transform (FFT) testing is to be performed on the

decimated record, then some integer number of cycles greater than one is usually desired. The input frequency, modified to provide exactly J cycles per record, is given by Equation (14)

$$f_i = nf_d + \frac{Jf_s}{M} \qquad N = 0, 1, 2, 3 \ldots \tag{14}$$

where J is the number of cycles in record of length M_d and the equivalent sampling rate f_{eq} is found by Equation (15):

$$f_{eq} = \frac{f_i M_d}{J} \tag{15}$$

Thus increasing J simultaneously increases the number of cycles in the decimated record and decreases the effective sampling rate. The parameter J is not necessarily an integer; it could be adjusted to give a non-integer number of cycles and exact integer equivalent sampling rate increases if that were desired.

4.1.3.4 Comments on alternate extraction method

This method uses simple keep-one-of-D samples decimation of the ADC output data stream to produce the equivalent-time data samples. Figure 7 depicts this operation. For $D = 2$, one ADC output sample is discarded, while the next is retained in the decimated record. If the decimation is done in software, then this method requires acquiring D times more ADC output samples than will be used. However, this method does not require complicated data reshuffling. Also, small frequency errors result in small errors in the equivalent sampling rate increase but do not result in apparent systematic jitter of the equivalent-time output samples. This method is useful when an ADC is to be characterized for operation near a given frequency. It does not yield exact integer times increase in effective sampling frequency.

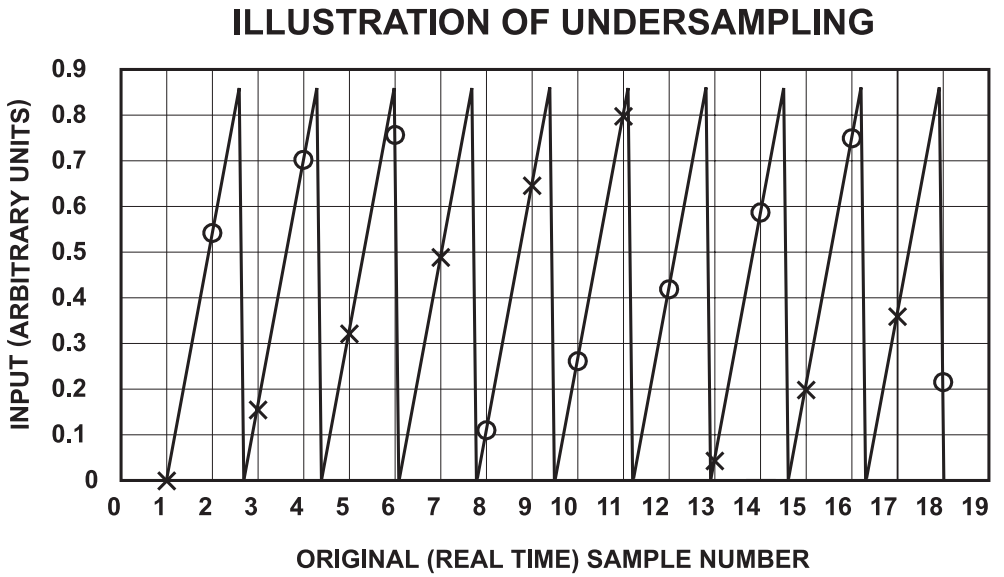

Figure 7—Continuous time waveform showing samples to be kept after decimation-by-2; samples marked "×" are kept; those marked "o" are discarded

This alternate extraction is a simple method for generating equivalent time records of arbitrary numbers of cycles per record which can utilize the same set of analog input frequencies required for coherent FFT-based tests. See 4.1.4.5 and 4.8.1 for coherent FFT input frequency discussions.

Specifically, when the integer M is a power of 2 and the integer D is also chosen to be a power of two, then the input frequencies chosen by Equation (14) will also be optimum input frequencies as

described by 4.1.4.5 when the parameter J is chosen to be an odd integer. It is thus possible to generate a coherent FFT of both the real-time signal and the equivalent-time signal from the same length M data record if this alternate extraction method is used with these restrictions upon M, D, and J.

As in any under-sampled application, small errors due to inclusion of undesired signals from the unwanted base band, or other aliases, may pollute the signal. For narrow band or sine signals the use of a bandpass filter at the ADC input minimizes any aliased artifacts.

One application of equivalent-time sampling is reconstructing an equivalent-time record to readily observe ADC anomalies, especially dynamic anomalies that become apparent only at input frequencies approaching or above the Nyquist frequency of the ADC. The equivalent-time record can also be used to measure settling times when a non-sinusoidal periodic waveform is used as the input signal. When the equivalent-sampling frequency is chosen to be much greater than the original sampling frequency the equivalent-time record can be used to measure settling times with much greater resolution. This is especially useful when the expected settling time is actually a fraction of one real-time sampling period

FFTs of the equivalent-time signal are normalized to the equivalent-sampling rate. This can be used to *unscramble* aliased harmonics. This eases the differentiation of harmonics from any spurious tones.

A numerical example clarifies the differences from the method of 4.1.3.1. With

sampling frequency	$f_s = 20\,\text{MHz}$
decimation factor	$D = 8$
decimated sample frequency	$f_d = 2.5\,\text{MHz}$
non-decimated record length	$M = 4096$
decimated record length	$M_d = 512$
number of cycles in M_d	$J = 1$

for $n = 1$, then

$f_i = 2.5\,\text{MHz}+20\,\text{MHz}/4096 = 2.5048828125\,\text{MHz}$
$f_{eq} = (2.5048828125\,\text{MHz})(512) = 1.2825\,\text{GHz}$
sampling rate increase $= 1.2825\,\text{GHz}/20\,\text{MHz} = 64.125$ times

for $n = 2$, then

$f_i = 5.0\,\text{MHz} + 20\,\text{MHz}/4096 = 5.0048828125\,\text{MHz}$
$f_{eq} = (5.0048828125\,\text{MHz})(512) = 2.5625\,\text{GHz}$
sampling rate increase $= 2.5625\,\text{GHz}/20\,\text{MHz} = 128.125$ times

4.1.4 Fitting sine waves

Some tests in this standard require estimates to determine parameters for a sine-wave model of ADC output samples in response to the sampling of an input sine wave. This clause describes two methods that are commonly used for data sets that may not represent an exact integer number of cycles, namely the three and four parameter fits. Subclause 4.1.5 discusses the DFT, which is usually used for the case where an exact integer number of input cycles are sampled.

Apply a sine wave with specified parameters to the input of the converter. Take a record of data. Fit a sine-wave function to the record by varying the phase, amplitude, dc value, and (if needed) frequency of the fit function to minimize the sum of the squared difference between the function and the data. Two suggested algorithms for least-squared fitting are given below, one for known frequency

solutions, when the ratio between the sample frequency and the input frequency is known and stable, and one for other cases.

4.1.4.1 Three-parameter (known frequency) least-squares fit to sine wave data using matrix operations

Assuming the data record contains the sequence of M samples $y_1, y_2, \ldots, y_M$, taken at times $t_1, t_2, \ldots, t_M$, this algorithm finds the values of A_0, B_0, and C_0 that minimize the following sum of squared differences [see Equation (16)]:

$$\sum_{n=1}^{M} \left[y_n - A_0 \cos(\omega_0 t_n) - B_0 \sin(\omega_0 t_n) - C_0\right]^2 \tag{16}$$

where ω_0 is the frequency applied to the ADC input.

To find the values for A_0, B_0, and C_0, first create Matrix (17), Matrix (18), and Matrix (19).

$$D_0 = \begin{bmatrix} \cos(\omega_0 t_1) & \sin(\omega_0 t_1) & 1 \\ \cos(\omega_0 t_2) & \sin(\omega_0 t_2) & 1 \\ . & . & . \\ . & . & . \\ \cos(\omega_0 t_M) & \sin(\omega_0 t_M) & 1 \end{bmatrix} \tag{17}$$

$$y = \begin{bmatrix} y_1 \\ y_2 \\ . \\ . \\ y_M \end{bmatrix} \tag{18}$$

$$x_0 = \begin{bmatrix} A_0 \\ B_0 \\ C_0 \end{bmatrix} \tag{19}$$

In matrix notation, the sum of squared differences in Equation (16) is given by that shown in Expression (20).

$$(y - D_0 x_0)^{\mathrm{T}} (y - D_0 x_0) \tag{20}$$

where $(*)^{\mathrm{T}}$ designates the transpose of (*).

Compute the least-squares solution, x_0, that minimizes Expression (20) using Equation (21).

$$x_0 = (D_0^{\mathrm{T}} D_0)^{-1} (D_0^{\mathrm{T}} y) \tag{21}$$

The fitted function is then given by Equation (22).

$$y_{n'} = A_0 \cos(\omega_0 t_n) + B_0 \sin(\omega_0 t_n) + C_0 \tag{22}$$

To convert the amplitude and phase to the form given in Equation (23).

$$y_{n'} = A \cos(\omega_0 t_n + \theta) + C \tag{23}$$

use Equation (24), Equation (25), and Equation (26).

$$A = \sqrt{A_0^2 + B_0^2} \tag{24}$$

$$\theta = \tan^{-1}\left[-\frac{B_0}{A_0}\right] \qquad \text{if } A_0 \geq 0 \tag{25}$$

$$\theta = \tan^{-1}\left[-\frac{B_0}{A_0}\right] + \pi \qquad \text{if } A_0 < 0 \tag{26}$$

The residuals, r_n, of the fit are given by Equation (27).

$$r_n = y_n - A_0\cos(\omega_0 t_n) - B_0\sin(\omega_0 t_n) - C_0 \tag{27}$$

and the root-mean-square (rms) error is given by Equation (28).

$$e_{\text{rms}} = \sqrt{\frac{1}{M}\sum_{n=1}^{M} r_n^2} \tag{28}$$

4.1.4.2 Comment on the relationship of the three-parameter fit to a discrete Fourier transform

In the special case where the frequency $f = \omega_0/2\pi$ is known and is an exact integer multiple J of f_s/M (i.e., there is an exact integer number J of cycles within the record), the three-parameter fit in 4.1.4.1 can be accomplished by performing a discrete Fourier transform (DFT) on the data record. A DFT computation can be relatively much faster, especially when it is implemented as a fast Fourier transform (FFT). If so, and if the first sample ($n = 0$) in the data record $y[n]$ is considered to be time zero, and the DFT of $y[n]$ is denoted by $Y[k]$, then the parameters of the three-parameter fit, A, θ, and C, in Equation (23) can be determined as shown in Equation (29), Equation (30), and Equation (31).

$$C = \frac{1}{M}Y[0] \tag{29}$$

$$A = \frac{2}{M}|Y[J]| \tag{30}$$

$$\theta = \tan^{-1}\left(\frac{\text{Im}\{Y[J]\}}{\text{Re}\{Y[J]\}}\right) \qquad \text{if } \text{Re}\{Y[J]\} > 0,$$

or

$$\theta = \left(\tan^{-1}\left(\frac{\text{Im}\{Y[J]\}}{\text{Re}\{Y[J]\}}\right) + \pi\right) \qquad \text{if } \text{Re}\{Y[J]\} < 0 \tag{31}$$

Also, the rms error (residuals) is given by Equation (32).

$$\varepsilon_{\text{rms}} = \frac{1}{M}\sqrt{\sum_{k\neq 0,J,M-J} |Y[k]|^2} \tag{32}$$

4.1.4.3 An algorithm for four-parameter (general use) least-squares fit to sine-wave data using matrix operations

Assuming the data record contains the sequence of M samples, $y_1, y_2, \ldots, y_M$, taken at times $t_1, t_2, \ldots, t_M$, this algorithm uses an iterative process to estimate the parameters A_i, B_i, C_i and ω_i, that minimize the sum of squared differences in Equation (33).

$$\sum_{n=1}^{M}[y_n - A_i\cos(\omega_i t_n) - B_i\sin(\omega_i t_n) - C_i]^2 \tag{33}$$

where ω_i is the frequency applied to the ADC input.

a) Set index $i = 0$. Make an initial estimate of the angular frequency ω_0 of the recorded data. The frequency may be estimated by using a DFT (on either the full record or a portion of it), or by

counting zero crossings, or simply by using the applied input frequency. Perform a pre-fit using the 3-parameter matrix algorithm given in 4.1.4.1 or 4.1.4.2 to estimate A_0, B_0, and C_0.

b) Set $i = i + 1$ for the next iteration.

c) Update the angular frequency estimate using Equation (34).

$$\omega_i = \omega_{i-1} + \Delta\omega_{i-1} \qquad (\Delta\omega_{i-1} = 0 \text{ for } i = 1) \tag{34}$$

d) Create Matrix (35), Matrix (36), and Matrix (37).

$$y = \begin{bmatrix} y_1 \\ y_2 \\ . \\ . \\ y_M \end{bmatrix} \tag{35}$$

$$D_i = \begin{bmatrix} \cos(\omega_i t_1) & \sin(\omega_i t_1) & 1 & -A_{i-1} t_1 \sin(\omega_i t_1) + B_{i-1} t_1 \cos(\omega_i t_1) \\ \cos(\omega_i t_2) & \sin(\omega_i t_2) & 1 & -A_{i-1} t_2 \sin(\omega_i t_2) + B_{i-1} t_2 \cos(\omega_i t_2) \\ . & . & . & . \\ . & . & . & . \\ \cos(\omega_i t_M) & \sin(\omega_i t_M) & 1 & -A_{i-1} t_m \sin(\omega_i t_M) + B_{i-1} t_m \cos(\omega_i t_M) \end{bmatrix} \tag{36}$$

$$x_i = \begin{bmatrix} A_i \\ B_i \\ C_i \\ \Delta\omega_i \end{bmatrix} \tag{37}$$

e) Compute the least-squares solution, x_i, as shown in Equation (38).

$$x_i = \left(D_i^{\mathrm{T}} D_i\right)^{-1} \left(D_i^{\mathrm{T}} y\right) \tag{38}$$

f) Compute the amplitude, A, and phase, θ, for the form in Equation (39).

$$y_{n'} = A\cos(\omega t_n + \theta) + C \tag{39}$$

using Equation (40)

$$A = \sqrt{A_i^2 + B_i^2} \tag{40}$$

and Equation (41) and Equation (42).

$$\theta = \tan^{-1}\left[-\frac{B_i}{A_i}\right] \qquad \text{if } A_i \geq 0 \tag{41}$$

$$\theta = \tan^{-1}\left[-\frac{B_i}{A_i}\right] + \pi \qquad \text{if } A_i < 0 \tag{42}$$

g) Repeat Steps b), c), d), e), and f), re-computing the model on the basis of the new values of A_i, B_i, and ω_i, calculated from the previous iteration. Continue to iterate until the changes in A, B, C, and ω are suitably small.

The residuals, r_n, of the fit are given by Equation (43).

$$r_n = y_n - A_i \cos(\omega_i t_n) - B_i \sin(\omega_i t_n) - C_i \tag{43}$$

and the rms error is given by Equation (44).

$$e_{\text{rms}} = \sqrt{\frac{1}{M}\sum_{n=1}^{M} r_n^2} \tag{44}$$

4.1.4.4 Comment on three-parameter versus four-parameter sine fit

The three-parameter sine fit algorithm of 4.1.4.1 (for the case of a known frequency) is a closed-form solution that will always produce an answer, but the answer will be a poorer fit than the four-parameter algorithm of 4.1.4.3 if the actual frequency applied to the ADC differs from the frequency used by the algorithm. The four-parameter fit, on the other hand, employs an iterative solution that may diverge for bad initial estimates, or especially corrupted data. Whichever method is used should be stated.

4.1.4.5 Comment on choice of input and clock frequencies, record size, and number of cycles per record

In sine-wave testing of ADCs, precise selection of the sampling clock and input sine-wave frequencies, and selection of the record size M, are very important. To evaluate an ADC's performance, it is desirable to maximize the number of distinct input phases that are sampled by the ADC, and if possible to get at least one representative sample from every ADC code. For an ideal ADC transfer characteristic in the absence of random noise, the minimum record size that would ensure a sample of every code bin is $M = \pi\ 2^N$, when the input sine-wave frequency is chosen as described below.

For a given sampling frequency there are certain input sine-wave frequencies which can conceal ADC errors, and other input sine-wave frequencies which will reveal ADC errors. These frequencies can differ by only a fraction of a percent. Input sine-wave frequency selection becomes more important as the input frequency is increased.

An optimum input sine-wave frequency is one for which there are M distinct phases which are uniformly distributed between 0 and 2π radians, where M is the number of samples in a record. It can be shown that the optimum frequencies are given by Equation (45)

$$f_{\text{opt}} = \left(\frac{J}{M}\right) f_{\text{s}} \tag{45}$$

where

J is an integer which is relatively prime to M,

f_{s} is the sampling frequency.

Note that the condition of being relatively prime means that M and J have no common factors and that for the optimum frequency there are exactly J cycles in a record. If M is a power of two, then any odd value for J meets this condition.

One example of a non-optimum frequency, which if used in testing may conceal ADC errors, is one for which Equation (46) is true.

$$f = \frac{f_{\text{s}}}{L} \tag{46}$$

where L is a small integer.

In this case there are only L distinct phases sampled.

Sometimes the optimum frequencies are too far apart to adequately approximate a desired input frequency. The following steps show a simple approach for calculating a near-optimum frequency which is close to any desired frequency.

a) Find an integer, r, such that the desired frequency is approximately f_s/r.

b) Let D [see Equation (47)] equal the number of full cycles that can be recorded at the frequency in Step a)

$$D = \text{int}\left(\frac{M}{r}\right) \tag{47}$$

c) Let f_i [see Equation (48)] equal the near-optimum frequency that will be the actual input frequency.

$$f_i = \frac{Df_s}{rD-1} \tag{48}$$

Using frequency f_i guarantees $(rD-1)$ distinct sampled phases uniformly distributed between 0 and 2π radians.

For example, if the sampling frequency is 1gigasample/second, the desired input frequency is 10 MHz, and the record length is 1024, then $r = 100$, $D = 10$ and $f_i = [10/999][1000] = 10.01001$ MHz. Using the frequency f_i guarantees 999 distinct uniformly distributed phases and differs from the desired frequency by only 0.1%. The nearest optimum frequency is $[11/1024][1000] = 10.742$ MHz. This differs from the desired frequency by 7.4% but guarantees 1024 distinct uniformly distributed phases. Using the desired frequency would yield only 100 distinct phases because its period is exactly 100 samples.

See also 4.1.5 for more on choosing record size, sample clock and sine-wave input frequencies, with respect to discrete Fourier transforms, windowing, and spectral leakage.

The number of cycles of the sine wave contained in the record also affects the estimates obtained from a sine fit. This is especially true for the four-parameter sine fit algorithm (see 4.1.4.3), in which frequency is not fixed. As the number of cycles in the record increases, the estimated frequency becomes more and more tightly constrained by the data, since the number of zero crossings increases. Therefore, for records containing large numbers of cycles, the sine fit will return frequency estimates that are very close to the fundamental frequency of the input signal. However, for records containing only a few cycles, e.g., less than 5, the estimated frequency is not strongly constrained by the fundamental frequency and therefore can also change to accommodate error components due to noise, harmonics, or jitter. The result is a fit that returns incorrect estimates, i.e., that do not exactly correspond to the parameters of the fundamental component of the signal, but nevertheless gives smaller mean squared error, and thus smaller residuals. Estimates of all four parameters—frequency, phase, amplitude, and offset—are affected. The differences in the estimates depend on the amount of noise, harmonics, and jitter present, as well as on the accuracy of the initial frequency estimate; if the signal is essentially free of contamination, the estimates will be quite good even for records containing only one cycle. A good rule of thumb is to use records containing at least five cycles. If the harmonics and noise are each less than $5Q$ (where Q is the ideal code bin width of the ADC), then the estimates will have sufficient accuracy for most applications.

4.1.5 Discrete Fourier transforms and windowing

In this standard, the discrete Fourier transform (DFT) is defined in 4.1.5.1 for a record of data $x[k]$ that is M samples long [see Equation (49)].

$$X[n] = \sum_{n=0}^{M-1} x[k] \times \exp(-j2\pi nk/M) \tag{49}$$

The inverse DFT is defined in Equation (50).

$$x[k] = \frac{1}{M} \sum X[n] \times \exp(+j2\pi kn/M) \tag{50}$$

In this standard, the inverse DFT includes the requisite $(1/M)$ normalization.

A windowed DFT is defined in Equation (51). The window factors, $w[k]$, filter the samples, $x[k]$, to conform to the required periodicity of the DFT sample time interval. The window functions are chosen in a trade-off between the effective noise bandwidth (ENBW), or resultant DFT bins, and minimum stop band response of the window filter function as discussed in 4.1.5.1.

$$Wx[n] = \sum_{n=0}^{M-1} w[k] \times x[k] \times \exp(-j2\pi nk/M) \tag{51}$$

4.1.5.1 Comments on windowing

Several test methods in this standard require the frequency transformation of a record of data using the DFT. These records often contain sinusoidal input signals, harmonics, intermodulation products, and other spurious signals that must be measured to characterize an ADC. The DFT of a data record will contain spectral components at frequencies other than those corresponding to each input frequency whenever the data record does not include an integer number of complete cycles of each input sinusoid. This is due to the fact that since the inverse DFT is a Fourier series at a fundamental frequency, f_s/M, it can only represent, or converge to, those signals that are fully periodic to f_s/M. These components, termed spectral leakage, are undesirable because they often mask spurious signals produced by the ADC. To properly characterize an ADC, choosing desirable input frequencies relative to the sampling rate of the ADC should minimize spectral leakage. It is desirable to use low-noise, high-precision signal sources whenever possible.

Choosing coherent sample clock and input sine-wave frequencies produces a frequency spectrum that exhibits single-line features corresponding to input frequencies and their nonlinear distortion products generated by the ADC. Choosing incoherent frequencies causes spectral leakage, which is manifest in the frequency spectrum as a spreading or *smearing* of spectral features corresponding to the input signal and any harmonic distortion products. The smearing yields inaccurate amplitude and phase estimates of components, and the smearing of larger spectral components obscures smaller spectral components. Where the use of incoherent frequencies is unavoidable, the application of a window weighting function to the sample sequence prior to frequency transformation can be used to reduce spectral leakage effects.

In practice, the use of window functions can usually be avoided by the careful selection of input signal frequencies and the use of high-precision input signal sources that are phase locked to a common clock or time reference. Ideally, the input signal frequency is chosen to satisfy two criteria:

a) The frequencies of all input test signals, f_i, are chosen to coincide exactly with DFT bins, m_i as shown in Equation (52).

$$f_i = \frac{m_i}{M} f_s \tag{52}$$

b) The DFT bins, m_i, corresponding to the input-signal frequencies are mutually prime with respect to the DFT length, M. Over a sufficient length of time, this condition permits all possible codes to be generated by the ADC. That is, the greatest common factor of the sample DFT bin and the DFT length should equal one, as shown in Equation (53).

$$\mathrm{GCF}(m_i, M) = 1 \tag{53}$$

Typically, the DFT is implemented as a fast fourier transform (FFT) where M is a power of two. For this case, the only factor of M is 2. Consequently, choosing m_i to be odd insures that the input signal cell and any FFT length are mutually prime.

In applying the DFT to process signals of finite-time duration, it may be necessary to apply a window function to the sample set if either of the following statements is true:

a) The input sine-wave source does not provide enough frequency precision and resolution to match the required frequency of the DFT bin. The frequency corresponding to the DFT bin is given by Equation (52). This may require that the sampling clock source and the signal source be phase locked using a reliable, temperature-controlled oscillator.

b) Phase noise present in the signal source or the signal clock generates spurious intermodulation products that are large enough in magnitude to dominate the spectral response, thereby limiting the noise-free dynamic range.

For the first case, a discrepancy between the input signal frequency and the frequency corresponding to the chosen DFT bin causes spectral leakage and spreading of spectral features. Multiplying the window function and the samples in the sequence time-domain minimizes these effects. This operation is equivalent to a convolution of the Fourier transform of each of the sequences, $x[n]$ and $w[n]$, in the frequency domain. The choice of the window to be applied to the sequence is heuristic. Often, however, window functions exhibiting low side lobes produce the most desirable results. A thorough treatment of window functions and their properties can be found in numerous texts (e.g., Harris [B13]; Oppenheim Schafer [B33]). Corrections to some of the windows presented in Harris [B13] and some additional windows with very low side lobes are presented in Nuttall [B31].

In the second case, the window's characteristic should be sufficient to minimize the deviation induced by random phase noise. A rule of thumb to ensure this is to choose a window function possessing side lobes at least 10 dB below the nominal noise floor of the ADC, which is determined by the ADC precision, the DFT length, and the equivalent-noise bandwidth of the window function [see Equation (54)].

$$\text{Noise floor (dBFS)} = 6.02N + 1.76 + 10\log_{10}\left(\frac{M}{2 \cdot \text{ENBW}}\right) \tag{54}$$

where M equals the window length in samples and N equals the number of ADC bits. The equivalent-noise bandwidth of the window function (Lindquist [B26]) is the average squared window weight divided by the mean window weight squared [see Equation (55)].

$$\text{ENBW} = \frac{M \sum_{k=0}^{M-1} w^2[k]}{\left(\sum_{k=0}^{M-1} w[k]\right)^2} \tag{55}$$

Here, k is the window coefficient index and $w[k]$ the window coefficient.

In summary, using a common oscillator to phase-lock low-phase-noise signal sources and the clock source, along with the judicious choice of the input-signal frequencies, will minimize the effects of spectral leakage. In practice, however, it may not be feasible to meet the preceding conditions. Therefore, the multiplication of a suitable window function together with a finite-length digital sequence produces a response where spectral leakage is significantly reduced. For this case, the fundamental and any spurious components produced by the ADC become observable as distinct lines in the spectrum.

4.1.6 Locating code transitions

In most cases, determining the code transition levels as discussed in 1.2 can represent the transfer characteristic of an ADC. Quantitatively, a code transition level is the value of the converter input parameter which causes half of the digital output codes to be greater than or equal to, and half less than, a given output code.

Note that it is not always possible to define a unique value for a particular code transition level. For instance, feedback from the output to the input of an ADC can cause either no, or a range of, input parameter values to cause an equal distribution of output codes on either side of a transition. See 4.1.7 for an alternate approach in these cases.

Once code-transition levels have been measured, then all static parameters, including integral and differential nonlinearity, missing codes, gain, and offset can be computed. There are three test methods in wide use: the feedback loop, the ramp histogram, and the sine wave histogram; they are described in the following subclauses.

4.1.6.1 Locating code transitions using a feedback loop

A widely used test method for determining transition levels is based on a feedback loop. In this method an input is applied to the ADC, the converter is triggered, and the results of the conversion are compared to a desired value. If the ADC output is below the desired value, the input is raised by a fixed amount. If the ADC output is equal to or above the desired value, the input is lowered by a fixed amount. This process is repeated until the ADC input has settled to a stable average value.

After the loop has settled, the input value can be either measured or, if the input source is well calibrated, computed from its transfer function.

4.1.6.1.1 Test method

A block diagram is given in Figure 8a. In this diagram, an N_{DAC}-bit digital-to-analog converter (DAC) generates the feedback signal, but other implementations are possible, including the classic analog one shown in Figure 8b. For clarity, we will discuss this method in terms of a DAC-generated input. In this test, N_1 and N_2 of Figure 8a are equal and assigned the value N_0. The DAC's value is decremented or incremented by N_0 after each conversion cycle according to the result of the comparison between the ADC's output code, k, and a designated reference code, k_{in}. Once the code transition level $T[k_{in}]$ has been reached, the feedback loop causes the input signal to oscillate across this transition in steps that can be chosen to be as small as desired down to the DAC resolution. The ADC input level is calculated from the known transfer function of the DAC, or is measured by an optional voltmeter.

In an ideal noiseless ADC, the asymptotic state of the test is an alternation between the values k_{in} and $k_{in}-1$, and the transition level is known only to an accuracy of N_0. Repeated tests with smaller values of N_0 can determine the transition level as precisely as desired.

In a real-world ADC, one with internal noise, the situation becomes more complex because the noise affects the properties of the asymptotic state of the test. Instead of a simple alternation about the desired code value, there will be a random walk about the transition level. The properties of this random walk depend on the relative values of the noise, the step size, and the code width. Choosing the optimum step size, N_0, is a tradeoff between speed of convergence and the desired accuracy. If N_0 is well chosen, this test is faster than either the histogram or the ramp techniques discussed in following clauses. The remainder of this discussion offers guidance in choosing the step size and the number of samples to be taken to achieve a desired accuracy.

In an ADC with no pipeline delay, N_0 would typically be set to the rms value of the converter noise. Converters with pipeline delay, P, would typically have N_0 set to the rms value of the noise divided by

$(P+1)$. Because this is a statistical process, the desired accuracy and the step size being used in the feedback loop determine the number of samples in the average. In general, there will be a setup period of M_1 samples, followed by an averaging period of M_2 samples. Optimizing the procedure requires some care in choosing M_1 and M_2. Papers by Max ([B29] and [B30]) give detailed guidance for doing this; this subclause gives rules of thumb for estimating values that work in most cases.

For the case where the step size, N_0, is greater than or equal to the noise, M_1 can be set to be eight. The initial DAC setting is assumed to differ from the true code edge by less than three times the rms value of the input noise of the ADC. This initial setting is usually evaluated by an input adjusting routine, which initially sets a large value for N_0, and eventually reduces the size of N_0 in binary steps to the point where the appropriate step size is reached for the final settling. If the step size is less than the noise level, the setup requires additional time. The number of setup samples is inversely proportional to the ratio of step size to noise value. For example, if the step size is one-half the noise value, M_1 should be sixteen; for one-quarter it would be thirty-two.

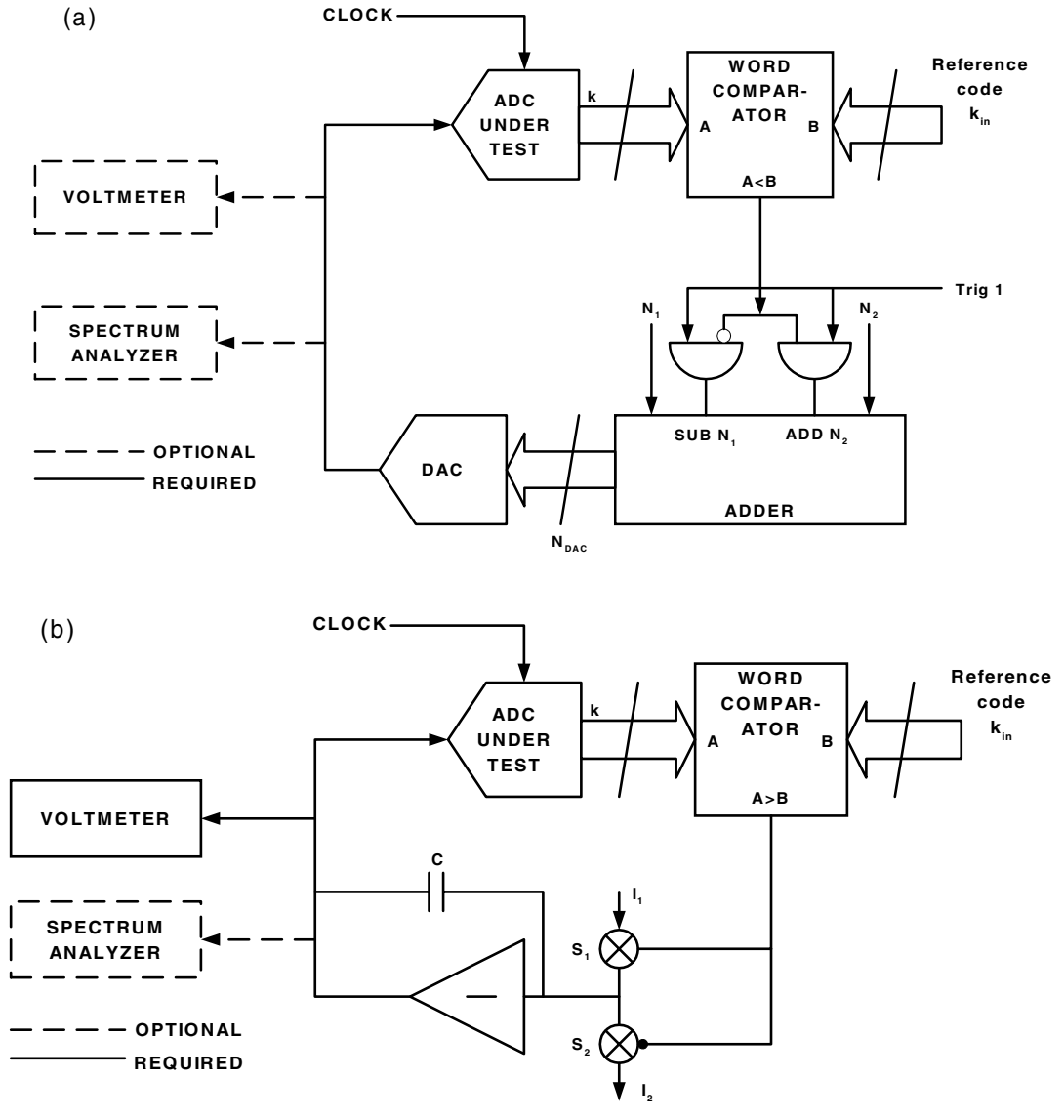

Figure 8—(a) Block diagram of feedback loop (digital method); (b) Block diagram of feedback loop (analog method)

Together, the desired accuracy of the noise measurement and the step size being used determine the choice of M_2. Figure 9 shows a plot that can be used for this purpose in most cases. For example, using this plot, one sees that at a step size corresponding to 0.5 output code widths and for a desired accuracy of 0.3 code widths, sixteen samples must be averaged. Users needing a more careful determination of M_2 are referred to Max [B29], and Max [B30].

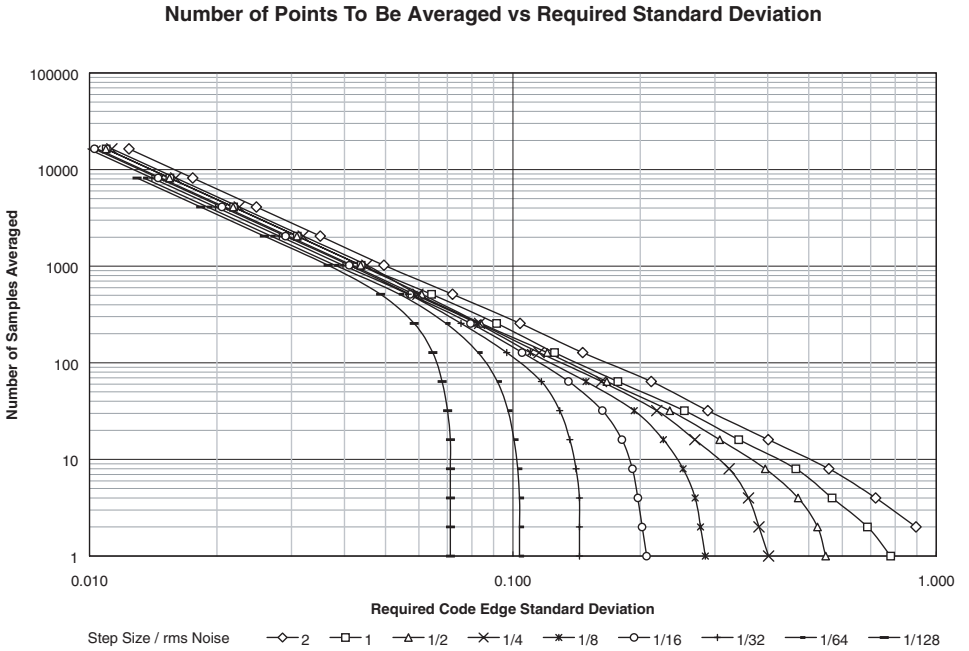

Figure 9—Number of points averaged versus required standard deviation

In principle, this technique can determine the shape of the noise at each code transition. This is beyond the scope of this standard and readers are referred to the papers given in Max [B29] and Max [B30].

4.1.6.2 Alternate code transition location method based on ramp histogram

In this approach, a histogram of code occurrences is generated in response to an input signal level which ramps linearly between the extremes of the full-scale range of the ADC. After a sufficiently large number of samples [determined from Equation (61)], the histogram of the output provides an accurate measure of the differential nonlinearity of the ADC. Integral nonlinearity can be directly computed by numerically integrating the differential nonlinearity data.

The input ramp should be generated synchronously with the sampling clock, by a high-resolution DAC or arbitrary waveform generator with suitable linearity. Absolute signal level measurements can be made at the terminal codes to compute offset and gain errors. The statistics of this process, as noted in the comments below, can be used to calculate how many hits per bin should be used to achieve a given confidence level based on the equivalent input noise level.

The location of the code transitions, $T[k]$, can be extracted by manipulating the data that is collected in a histogram test with a ramp input. The code transition levels are given by Equation (56)

$$T[k] = C + A \cdot H_c[k-1] \qquad \text{for } k = 1, 2, \ldots, (2^N - 1) \tag{56}$$

where

A is a gain factor,

C is an offset factor,

$H_c[j]$ is equal to $\sum_{i=0}^{j} H[i]$,

$H[i]$ is the number of histogram samples received in code bin i,

S is equal to $\sum_{i=0}^{2^N-1} H[i]$ = the total number of histogram samples.

The values of C and A can be computed directly from the collected data and the direct measurement of $T[1]$ and $T[2^N-1]$. The expressions for A and C are given by Equation (57) and Equation (58).

$$A = \frac{\left(T[2^N - 1] - T[1]\right)}{(S - H[2^N - 1] - H[0])} \tag{57}$$

$$C = T[1] - \left(\frac{H[0] \times \left(T[2^N - 1] - T[1]\right)}{(S - H[2^N - 1] - H[0])}\right) \tag{58}$$

It should be noted that if code bins 0 and 2^N-1 are excluded (defined as having zero width) then the expressions reduce to Equation (59) and Equation (60).

$$A = \frac{\left(T[2^N - 1] - T[1]\right)}{S} \tag{59}$$

$$C = T[1] \tag{60}$$

4.1.6.2.1 Comments on number of samples to be averaged per transition level for a given confidence level

The precision of the measured values of the code transition levels depends on the total number of histogram samples measured. Increasing the number of samples decreases the uncertainty while ramping the input. The larger the total, the lower the uncertainty. Nonlinearity of the ramp input signal would produce errors in the code transition levels. Noise on the ramp signal or the ADC under test will cause uncertainty in the measured code transition levels. Specifically, the uncertainty in LSBs due to noise in the estimate of a transition level is approximated by Equation (61).

$$\varepsilon \approx \sqrt{\frac{\sigma}{H}} \tag{61}$$

where

σ is the standard deviation of the noise, in units of ideal code bin widths (LSBs),

H is the average number of histogram samples received in each of the code bins that share the given transition level.

4.1.6.2.2 Comments on ramp characteristics

The ramp method is generally used when static characteristics of the device under test are being measured. The sine-wave histogram is generally used for dynamic testing. The ramp method is more efficient in measuring the device characteristics.

4.1.6.2.3 Comments on histogram testing

Histogram methods can produce erroneous results if the device being tested has output codes that are swapped with other codes or exhibits other types of non-monotonic behavior. Such converters can produce seemingly good results, yet have large errors in the actual code transitions. To avoid these issues, converters should also be tested for SINAD performance to confirm that non-monotonic behavior is not significant.

4.1.6.3 Alternate code transition location method, based on sine-wave histogram

This method of locating code transitions is often easier to implement than the prior one, especially if one is interested only in determining nonlinearities. A pure sine wave of amplitude sufficient to slightly overdrive the ADC is input to the ADC under test. The frequency of the sine wave and the ADC sampling frequency shall be specified. Multiple records of ADC output data are taken and a histogram constructed. Selection of the sine-wave frequency, the number of samples per record, and the number of data records taken are discussed in 4.1.6.3.1 and 4.1.6.3.2. If the input range of the ADC is not symmetrical around the middle of the full-scale range, then a constant must be added to the sine wave so that the peaks of the combined signal are equidistant from the center of the full-scale range. The amount of overdrive required depends on the combined noise of the input signal and the ADC additive noise. If the amplitude and offset of the sine wave are precisely known, this method gives the transition levels to the same precision. If the amplitude of the sine wave and the offset are unknown, this method gives the transition levels to within a gain and offset error; i.e., the calculated transition levels, $T'[k]$, will be related to the true transition levels, $T[k]$, by the relation in Equation (62)

$$T'[k] = a \times T[k] + b \tag{62}$$

where a and b are constants.

This test assumes that the ADC is monotonic and has no hysteresis. See 4.4.3 and 4.4.4 for definitions of these terms.

The sine-wave frequency must be chosen as described below in 4.1.6.3.1. Note that different frequencies may produce different results, due to dynamic errors.

Take many records of data (the required amount is covered in 4.1.6.3.2) and keep track of the total number of samples received in each code bin. The transition levels are then given by Equation (63)

$$T[k] = C - A\cos\left[\frac{\pi \times H_c[k-1]}{S}\right] \qquad \text{for } k = 1, 2, \ldots, (2^N - 1) \tag{63}$$

where

A is the amplitude of the sine wave,

C is the offset (dc level) of the applied signal,

$H_c[j]$ is equal to $\sum_{i=0}^{j} H[i]$,

$H[i]$ is the total number of samples received in code bin i,

S is the total number of samples.

If A and C are unknown, they can be determined from the data and an independent estimate of any two of the transition levels $T[k]$. Errors in the values of A and/or C do not induce any errors in the determination of differential or integral nonlinearity from the calculated transition levels because they only induce gain and offset errors in the transition levels, as shown in Equation (62). These results are derived in Vanden Bossche et al. [B44].

This test assumes that the transfer function is monotonic (see 4.4.3).

4.1.6.3.1 Comment on the selection of the sine-wave frequency and data record length

The frequency of the sine wave and the record length of the data collected must be carefully selected in order for the error estimates of the preceding subclause to apply. There must be an exact integer number, J, of cycles in a record, and the number of cycles in a record must be relatively prime to the number of samples in the record. This guarantees that the samples in each record are uniformly distributed in phase from 0 to 2π.

If the test frequency is low enough that dynamic errors do not arise, this method will give the same results as the static test method. If the frequency is chosen large enough that the dynamic errors are significant, the user should be warned that some dynamic errors will appear in the results while others will be averaged out by the histogram calculations.

A frequency that meets the above requirements, can be selected as follows. Choose the number of cycles per record, J, and a record length, M, such that J and M have no common factors. Choose the frequency using Equation (64).

$$f_i = \frac{J}{M} f_s \tag{64}$$

where

f_i is the input signal frequency,

f_s is the sampling frequency.

In order for the test tolerances in the derivations in 4.1.6.3.2 to be valid, the accuracy required of the ratio of the input signal frequency to the sampling frequency is given by Equation (65).

$$\frac{\Delta a}{a} \leq \frac{1}{2JM} \tag{65}$$

where

$$a \equiv \frac{f_i}{f_s} \tag{66}$$

With larger values of M, fewer total samples (the number of records times the number of samples per record) will be required to obtain any given accuracy, but greater accuracy will be required of the signal frequency. The best approach is to use the largest value of M compatible with the frequency accuracy obtainable. The frequency accuracy specified by Equation (65) and Equation (66) guarantee that the phase separation between samples is within $\pm$ 25% of the ideal. This tolerance is assumed in the derivation of Equation (67).

4.1.6.3.2 Comments on histogram testing

The same testing inaccuracies can occur in sine-wave histogram testing that are indicated in 4.1.6.2.3. Again, to avoid these issues, converters should also be tested for SINAD performance to confirm that non-monotonic behavior is not significant.

4.1.6.3.3 Comment on the amount of overdrive and the number of records required

The minimum amount of overdrive required in the method in 4.1.6.3 depends on the combined noise level of the signal source and the ADC. In the absence of noise, the overdrive need only be sufficient to receive at least one count in each of the first and last code bins. If noise is present, it will modify the probabilities of samples falling in various code bins, and the effect will be largest near the peaks where the curvature of the probability density is greatest. This effect can be made as small as desired by making the overdrive large enough. The amount of overdrive required to obtain a specified accuracy also depends on whether the specified accuracy is for the code bin widths (i.e., differential nonlinearity) or for the transition levels (i.e., integral nonlinearity).

Input overdrive

The overdrive required to obtain a specified tolerance in code bin widths is given by Equation (67).

$$V_o \geq \text{Maximum of } (3\sigma) \text{ or} \left(\sigma \times \sqrt{\frac{3}{2B}} \right) \tag{67}$$

where

σ is the rms value of the random noise in input units,

B is the desired tolerance as a fraction of the code bin width,

V_o is the input overdrive: the difference between the positive (negative) peaks of the sine wave and the most positive (negative) transition level of the ADC.

This amount of overdrive guarantees that the error caused by the noise is $\leq 1/3$ of the desired tolerance.

The overdrive required to obtain a specified tolerance in transition levels is given by Equation (68).

$$V_o \geq \text{Maximum of } (2\sigma) \text{ or } \frac{\sigma^2 2^N}{FSRB} \tag{68}$$

where

V is the full-scale range of the instrument in input units,

N is the number of bits of the ADC.

The values of V_o in Equation (67) and Equation (68) are adequate to keep the errors due to noise equal to or less than $B/3$ code bin widths so that these errors are negligible when added to the statistical errors due to taking a finite number of samples.

The number of records required depends on several factors. It depends on the combined noise level of the ADC and the signal source, on the desired test tolerance and confidence level, on whether the tolerance and confidence level is for INL (transition levels) or DNL (code bin widths) and on whether one wants to obtain the desired confidence for a particular width or transition level or for the worst case for all widths or transition levels. The number of records required for a given test tolerance and a given confidence in code bin widths is given by Equation (69).

$$R = D \times \left[\frac{2^{(N-1)} K_u}{B}\right]^2 \times \left[\frac{c\pi}{M}\right] \times \left\{1.13\left[\frac{\sigma^*}{V} + \frac{c}{2}\sigma_\phi\right] + 0.25\left[\frac{c\pi}{M}\right]\right\} \tag{69}$$

where

R is the minimum required number of records,

D is equal to 1 for INL and $D = 2$ for DNL,

M is the number of samples per record,

c is equal to $1 + 2(V_o/V)$,

V is the full-scale range of the ADC under test,

V_o is the input overdrive,

K_u is equal to $Z_{u/2}$ for obtaining the specified confidence in an individual transition level or code bin width,

K_u is equal to $Z_{N,u/2}$ for obtaining the specified confidence in the worst-case transition level or code bin width,

u is equal to $1-v$, with v the desired confidence level expressed as a fraction,

σ^* is for INL, σ, the rms random noise effects including additive noise and jitter,

σ^* is for DNL, the minimum of σ or $Q/2.26$,

$\sigma\pi$ is the rms random phase error of the input signal relative to the sampling time, in radians,

N is the number of bits of the ADC,

B is the desired test tolerance as a fraction of the code bin width.

The values for $Z_{u/2}$ and $Z_{N,u/2}$ can be obtained from Table 2. For values of N between those in the table, use linear interpolation. $Z_{u/2}$ is defined such that the probability is $(1-u)$ that the absolute value of a Gaussian distributed random variable, having a mean of zero and a standard deviation of one, is less than or equal to $Z_{u/2}$. $Z_{N,u/2}$ is defined such that the probability is $(1-u)$ that the maximum of the absolute values of 2^N Gaussian distributed random variables, having means of zero and standard deviations of one, will be less than or equal to $Z_{N,u/2}$.

Table 2—Values of $Z_{u/2}$ and $Z_{N,u/2}$

u	$Z_{u/2}$	$Z_{4,u/2}$	$Z_{8,u/2}$	$Z_{12,u/2}$	$Z_{16,u/2}$	$Z_{20,u/2}$	$Z_{24,u/2}$
0.2	1.28	2.46	3.33	4.04	4.64	5.19	5.68
0.1	1.64	2.72	3.53	4.21	4.80	5.33	5.81
0.05	1.96	2.95	3.72	4.37	4.94	5.46	5.93
0.02	2.33	3.22	3.95	4.57	5.12	5.62	6.08
0.01	2.58	3.42	4.11	4.71	5.25	5.74	6.19
0.005	2.81	3.60	4.27	4.85	5.38	5.85	6.30
0.002	3.09	3.84	4.47	5.03	5.54	6.01	6.44
0.001	3.29	4.00	4.62	5.16	5.66	6.12	6.54

Equation (64), Equation (65), Equation (66), Equation (67), and the values in Table 2, are derived in Blair [B4]. For further information, see Papoulis [B35].

4.1.7 Determining the static transfer curve

The transfer curve of an ADC is the average output code, $\bar{y}$, as a function of a particular input signal level, x. The transfer curve, $\bar{y}(x)$, is used as a basis for alternate definitions of many of the static parameters of an ADC, e.g., gain and offset, INL, monotonicity, etc. The transfer curve (and the parameter definitions based on it) is especially useful in specifying ADCs where it may be impractical or impossible to measure the code transition levels. Examples of such ADCs are those with a high number of digitized bits (it may be impractical to search for all 2^{20} code transition levels for a 20-bit ADC), those with non-monotonic behavior and/or output-to-input crosstalk (which can result in either undefined or multiply-defined code transition levels), and those ADCs that are actually composed of multiple time-interleaved sample-holds and/or ADCs.

Another useful measurement that can be made at the same time as the transfer curve is the deviation of the output codes about the average, again as a function of the input signal value, x.

To estimate the transfer curve, $\bar{y}(x)$, and the standard deviation of the output as a function of the input, $\sigma_y(x)$, a dc input source is required whose output signal range spans slightly more than the

full-scale range of the ADC, and that has an accuracy, resolution, and noise better than the desired accuracy of the measurement.

a) Set the level of the input signal, x, slightly below the bottom of the ADC input range (such that further lowering of the input level would not change the ADC output).

b) Acquire M samples from the ADC: $y_0, y_1, y_2, \ldots, y_{M-1}$. M should be chosen large enough that the standard deviation of the sample mean (the standard deviation of the samples divided by the square root of M) is small compared to the desired accuracy of the measurement.

c) Record the sample mean (estimated average), $\bar{y}(x)$, and standard deviation, $\sigma_y(x)$, of these M samples in arrays indexed by the current input level x.

d) Increment the input level x by a specified amount. Preferably, the increment is roughly equal to the deviation of the additive random noise present within the ADC at the analog input, or $Q/8$, whichever is larger.

e) Repeat steps b, c, and d until the input level x is set slightly above the top of the ADC input range (such that further raising of the input level would not change the ADC output).

4.1.7.1 Alternate method

The order of the loops in the above method (the inner loop being the acquisition of M samples in Step (b) may be reversed. In this case, the input signal becomes a repetitive ramp, increasing by the specified amount per sample interval. M records of data are acquired, each record triggered so as to contain points digitized from when the ramp was set at a specific point slightly below the bottom of the ADC input range to when the ramp was slightly above the top of the range. The M records are then compared on a point-by-point basis to find the mean and deviation.

Both techniques can also be used with a decreasing rather than increasing input level. If the results differ significantly (e.g., due to hysteresis), the transfer curve is the average of the results using an increasing and a decreasing input level.

4.2 Analog input

4.2.1 Input impedance

The minimum specification for input impedance is the static input resistance and, if significant, the input capacitance and inductance.

4.2.1.1 Static input resistance

The static input resistance is the ratio of the change of an applied static input signal to the resulting (static) change of input current. If the best model of the ADC includes a significant current source, it should be specified.

4.2.1.2 VSWR and reflection coefficient

VSWR is the ratio of the mismatch between the actual impedance and the desired or expected impedance. It can be calculated by measuring the reflection coefficient of the ADC input terminal through application of a test signal. The reflection coefficient, ρ, of a simple terminating impedance, Z_t, is given by Equation (70).

$$\rho = \frac{Z_t - Z_0}{Z_t + Z_0} \tag{70}$$

where

Z_t is the ADC input termination impedance,

Z_0 is the transmission line impedance, nominally 50 Ω.

VSWR [as shown in Equation (71)] becomes

$$\text{VSWR} = \frac{1 + |\rho|}{1 - |\rho|} \tag{71}$$

To measure the reflection coefficient, ρ, connect a vector impedance meter of desired accuracy and appropriate output signal to the ADC input using the circuit in Figure 10. To select the most accurate measurement circuit, the approximate ADC input impedance should be known. When available, calibration standards (typically short, open, and 50 ohm standards) should be used to correct for circuit inaccuracies in the measurement. [as shown in Equation (71)]

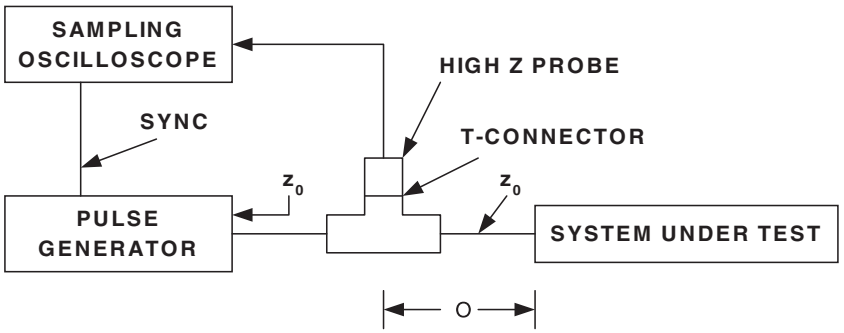

Figure 10—Circuit for measuring the reflection coefficient

4.2.1.3 Alternate test methods

Many more measurement methods and circuits may be used, solely or in combination, to achieve more applicable impedance range measurements or accuracy of the same. Some to consider are bridge method, resonant method, I–V method, network analysis method, time domain network analysis method, and the auto-balancing bridge method. These methods, their circuits, advantages and disadvantages are outlined in Honda [B14].

4.2.1.4 Comment on input impedance measurements

VSWR or input impedance should, as a minimum, be characterized for the ADC analog input pin(s) and the encode/clock pin(s) as these pins easily influence the overall testing accuracies. Mismatches between the ADC pins and the instrumentation connected to them for testing will cause unnecessary errors to be introduced into the measurement system. Reflections can also occur on the output digital code word lines which are likely to couple back into the pure input sine waves, causing distortion and noise. Proper impedance matching and/or attenuation and isolation of these output signal lines will give superior test results.

4.2.2 Static input impedance versus input signal level

Some devices may vary in input impedance over the specified operating range of input signal levels. Perform the test in 4.2.1 with the input signal level set at a minimum of three equally spaced signal levels over the range of the device. Measure the impedance at each of the input settings as defined in 4.2.1.

4.2.2.1 Test method

Connect a vector impedance meter of desired accuracy and appropriate output level to the device. Vary the frequency over the desired range and record results. Note that if a test fixture is used which can affect the measurement the construction details of the fixture should be stated as well as the results obtained in the fixture. Any readings obtained in the fixture should be recomputed to remove the effect of the fixture.

4.2.3 Static input current

Apply a series of three equally spaced signal levels across the maximum useable input range of the device. Measure the current entering the device, using an appropriate current meter for each of the signal levels.

4.3 Static gain and offset

Static gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to minimize the mean squared deviation from the output values. For static measurement of gain, see 4.3.1 and 4.3.2. Unless otherwise specified in this standard, static gain and offset will be taken to mean independently based gain and offset measured as in 4.3.1. For dynamic measurement of gain, see 4.7.3.

4.3.1 Static gain and offset (independently based)

Independently based static gain and offset are the values by which static input values are multiplied and then to which the input values are added, respectively, to minimize the mean squared deviation from the output values. Unless otherwise specified, static gain and offset will be taken to mean independently based static gain and offset. Test method: Locate the code transition levels as per 4.1.6. The transfer characteristic can then be represented by Equation (72).

$$G \times T[k] + V_{os} + \varepsilon[k] = Q \times (k-1) + T_1 \tag{72}$$

where

$T[k]$ is the input value corresponding to the transition between codes k and $k-1$,

T_1 is the ideal value corresponding to $T[1]$,

V_{os} is the output offset in units of the input quantity, nominally equal to zero,

G is the gain, nominally equal to unity,

Q is the ideal width of a code bin, that is, the full-scale range divided by the total number of codes,

$\varepsilon[k]$ is the residual error corresponding to the kth code transition.

The expression on the right side of Equation (72) gives the ideal code transition level, in input units, as a function of k. The variable, k, is assumed to be the value of the binary coded output. Using conventional linear least-squares estimation techniques, independently based static offset and gain are the values of V_{os} and G that minimize the mean squared value of $\varepsilon[k]$ over all k. The value of G that

minimizes the mean squared value of $\varepsilon[k]$ is given by Equation (73).

$$G = \frac{Q(2^N - 1)\left(\sum_{k=1}^{2^N-1} kT[k] - 2^{(N-1)}\sum_{k=1}^{2^N-1} T[k]\right)}{(2^N - 1)\sum_{k=1}^{2^N-1} T^2[k] - \left(\sum_{k=1}^{2^N-1} T[k]\right)^2} \tag{73}$$

and the value of V_{os} that minimizes the mean squared value of $\varepsilon[k]$ is shown in Equation (74).

$$V_{os} = T_1 + Q(2^{(N-1)} - 1) - \frac{G}{(2^N - 1)}\sum_{k=1}^{2^N-1} T[k] \tag{74}$$

Given these values for G and V_{os}, $\varepsilon[k]$ is the independently based integral nonlinearity (see 4.4.1).

4.3.1.1 Alternate method for determining gain and offset

The independently based static gain and offset may alternatively be found by using a least-squares fit of a straight line to the transfer curve (see 4.1.7). In order to avoid having the ends of the transfer curve, where the ADC is overdriven, affect the fit, the straight line is fitted just to that portion of the transfer curve where the average output code is between its minimum value plus twice its deviation and its maximum value minus twice its deviation. This method may give slightly different results to those of the fit of straight line to the code transition levels, but the differences are insignificant in practical cases.

4.3.2 Static gain and offset (terminal-based)

Static terminal-based gain and offset are the values by which static input values are multiplied and then to which the input values are added, respectively, to cause the deviations from the output values to be zero at the terminal points, that is, the first and last codes.

Test method: Locate the code transitions as per 4.1.6. The transfer characteristics can be represented by Equation (72). Terminal based static gain and offset are the values of G and V_{os} that cause $\varepsilon[1] = 0$ and $\varepsilon[2^N - 1] = 0$, where N is the number of digitized bits and $2^N - 1$ is the highest code transition defined.

4.4 Linearity

4.4.1 Integral nonlinearity

The integral nonlinearity is the difference between the ideal and measured code transition levels after correcting for static gain and offset. Integral nonlinearity is usually expressed as a percentage of full scale or in units of LSBs. It will be independently based or terminal-based depending on how static gain and offset are defined. When the integral nonlinearity is given as one number without code bin specification, it is the maximum integral nonlinearity of the entire range.

4.4.1.1 Integral nonlinearity test method

Find the static gain and offset per method 4.3.1 or 4.3.2, as appropriate for independently based or terminal based static gain and offset. The static integral nonlinearity as a function of k is given in percent by Equation (75)

$$\mathrm{INL}[k] = 100\% \times \frac{\varepsilon[k]}{2^N \times Q} = 100\% \times \frac{\varepsilon[k]}{V_{FS}} \tag{75}$$

where

INL(k) is the integral nonlinearity at output code k,

$\varepsilon[k]$ is the difference between $T[k]$ and ideal value of $T[k]$ computed from G and V_{os},

Q is the ideal code bin width, expressed in input units,

V_{FS} is the full-scale range of the ADC in input units.

The maximum INL is the maximum value of $|\text{INL}[k]|$ for all k.

4.4.1.2 Alternate test method for determining INL

An alternative method can determine INL from the transfer curve. This is useful in cases where the code transition levels are difficult or impossible to determine, e.g., when the ADC is actually a set of interleaved ADCs. To use this method, first determine the transfer curve according to 4.1.7. Then smooth it with a *boxcar* function of width Q, centered on zero, and with an area of one. This creates a running average of length Q. The INL is the maximum absolute deviation of the smoothed transfer curve from the best-fit straight line as found in determining gain and offset in 4.3.1.1. The search for the maximum is taken over the same range of input levels as used to fit the straight line in 4.3.1.1. Because of this, this test method may not find the worst-case INL if it occurs within twice the deviation of the first or last transition level.

4.4.2 Differential nonlinearity and missing codes

Differential nonlinearity (DNL) is the difference, after correcting for static gain, between a specified code bin width and the ideal code bin width, divided by the ideal code bin width. When given as one number without code bin specification, it is the maximum differential nonlinearity of the entire range. It is given in Equation (76).

$$\text{DNL}[k] = (W[k] - Q)/Q \tag{76}$$

where

$W[k]$ is the width of code bin k, $T[k+1]-T[k]$,

Q is the ideal code bin width,

G is the static gain.

Neither the width of the top bin, $W[2^N-1]$, nor that of the bottom bin, $W[0]$, is defined. A code k is defined to be a missing code if Equation (77) is true.

$$\text{DNL}[k] \leq -0.9 \tag{77}$$

Perfect differential nonlinearity coincides with $\text{DNL} = 0$.

The maximum differential nonlinearity is the maximum value of $|\text{DNL}[k]|$ for all k. In addition, the RMS value of the DNL can be given as shown in Equation (78).

$$\text{DNL}_{\text{RMS}} = \left(\frac{1}{2^N - 2} \sum_{k=1}^{2^N-2} \{\text{DNL}[k]\}^2 \right)^{1/2} \tag{78}$$

4.4.3 Monotonicity

A monotonic non-inverting ADC produces output codes that are consistently increasing with increasing input stimulus and consistently decreasing with decreasing input stimulus, changing in the same direction relative to the change in input stimulus. If the input stimulus and output codes change consistently in opposite directions, e.g., a higher input produces a lower output code, the ADC is monotonic and inverting.

4.4.3.1 Test method

Determine the transfer curve of the ADC using both increasing and decreasing input levels, according to 4.1.7. Then the ADC is considered non-monotonic if, for any pair of input levels x_1 and x_2, with $x_1 < x_2$ as shown in Equation (79) and Equation (80).

$$\bar{y}(x_1) - \frac{3 \times \sigma_y(x_1)}{\sqrt{M}} > \bar{y}(x_2) + \frac{3 \times \sigma_y(x_2)}{\sqrt{M}} \quad \text{(non-inverting)} \tag{79}$$

$$\bar{y}(x_2) - \frac{3 \times \sigma_y(x_2)}{\sqrt{M}} > \bar{y}(x_1) + \frac{3 \times \sigma_y(x_1)}{\sqrt{M}} \quad \text{(inverting)} \tag{80}$$

using the notation of 4.1.7, where $\bar{y}(x)$ is the mean output code value and $\sigma_y(x)$ is the standard deviation of the output code value, for a given static input signal level x, and M is the number of samples taken at each x value. Note that it is best to keep $M > 20$ to assure that the standard deviation estimates $\sigma_y(x_1)$ and $\sigma_y(x_2)$ are statistically valid.

4.4.4 Hysteresis

The measured value of the ADC transfer curve may depend on the direction by which the transfer curve is traversed (i.e., increasing or decreasing signal). The reported hysteresis of the ADC, if any, is the maximum of such differences.

4.4.4.1 Hysteresis test method

Determine the transfer curve of the ADC using both increasing and decreasing input levels (see 4.1.7). Let $\bar{y}+(x)$ and $\bar{y}-(x)$ denote the mean output values measured at input level x for increasing and decreasing input levels, respectively, and let $\sigma_{y+}(x)$ and $\sigma_{y-}(x)$ be the calculated standard deviation of those measured values, for increasing and decreasing input levels, respectively. Let $M_+(x)$ and $M_-(x)$ be the number of measurements of the output value at input value x, for increasing and decreasing input values, respectively.

If, for all levels x, the difference between the measured mean ADC output values for increasing and decreasing input levels is within the random measurement uncertainty, i.e., if Equation (81) is true.

$$|\bar{y}_+(x) - \bar{y}_-(x)| \le 3 \times \left| \left(\frac{\sigma_{y+}(x)}{\sqrt{M_+(x)}} \right)^2 - \left(\frac{\sigma_{y-}(x)}{\sqrt{M_-(x)}} \right)^2 \right|^{1/2} \tag{81}$$

then the ADC is said to have no hysteresis. Note that it is best to keep M_+ and M_- greater than about 20, to assure that the standard deviation estimates are statistically valid. If the ADC does have hysteresis, the amount is given by the magnitude of the largest observed difference, converted to the units of the input signals. Thus in Equation (82)

$$\text{hysteresis} = \frac{|\bar{y}_+(x) - \bar{y}_-(x)|_{\max}}{G} \tag{82}$$

4.4.4.2 Alternate hysteresis test method

Another method of measuring ADC hysteresis, using a feedback loop, is described in 4.5.3.3. There, the magnitude of the hysteresis at the code transition level of interest is converted into the position of a peak in a frequency spectrum, which is measurable with a spectrum analyzer.

4.4.5 Harmonic and spurious distortion

Dynamic errors and integral nonlinearities contribute to harmonic distortion whenever an ADC is sampling a periodic signal. This clause describes different measures that are used to quantify such behavior.

For a pure sine wave input, the output harmonic distortion components are found at spectral values whose non-aliased frequencies are integer multiples of the applied sine wave frequency. Their amplitudes, which depend upon the amplitude and frequency of the applied sine wave, are generally given as a decibel (dB) ratio with respect to the amplitude of the applied sine wave input. Their frequencies are usually expressed as a multiple of the frequency of the applied sine wave. For pure sine wave input, spurious or non-harmonic components are persistent sine waves at frequencies other than the fundamental (input) or those described above as harmonic components. Usually, their amplitudes are expressed as a dB ratio with respect to a full-scale signal (dBFS).

The measures described in the following clauses derive from the use of a spectrally pure, large amplitude sine wave input as the test signal. The test signal should be properly filtered to lower all harmonics to a level that is well below the desired measurement resolution for the device under test. The amplitude and frequency of the test signal shall be specified in the test results.

4.4.5.1 Total harmonic distortion

Total harmonic distortion (THD) is the square root of the sum of squares of a specified set of harmonic distortion components including their aliases.

To estimate THD, calculate the root sum of squares of the specified subset of harmonics, f_h, as shown in Equation (83).

$$\mathrm{THD} = \frac{1}{M}\sqrt{\sum_h \left(X_{\mathrm{avm}}(f_h)\right)^2} \tag{83}$$

where

$X_{\mathrm{avm}}(f_h)$ is the averaged magnitude of the component at the hth harmonic of the DFT of the ADC output data record

M is the number of samples in the data record.

The members of the set of harmonics, f_h, used in Equation (83), must be specified. The choice of harmonic components included in the set is a tradeoff between the desire to include all harmonics with a significant portion of the harmonic distortion energy, but not to include DFT bins whose energy content is dominated by random noise. Unless otherwise specified, to estimate THD, the set is normally composed of the lowest nine harmonics, 2nd through 10th inclusive, of the input sine wave. The percent total harmonic distortion is computed by comparing the THD estimate to the rms of the output fundamental component at the signal test frequency, $f_{\mathrm{i}} = Jf_{\mathrm{s}}/M$, as shown in Equation (84) and Equation (85).

$$\%\mathrm{THD} = \left(\frac{\mathrm{THD}}{A_{\mathrm{rms}}}\right) \times 100\% \tag{84}$$

$$A_{\mathrm{rms}} = \frac{1}{M}\sqrt{\left(X_{\mathrm{avm}}(f_{\mathrm{i}})\right)^2 + \left(X_{\mathrm{avm}}(f_{\mathrm{s}} - f_{\mathrm{i}})\right)^2} \tag{85}$$

The THD is also often expressed as a dB ratio with respect to rms amplitude of the fundamental component of the output, as shown in Equation (86).

$$\mathrm{THD}_{\mathrm{dB}} = 20\log_{10}\left(\frac{\mathrm{THD}}{A_{\mathrm{rms}}}\right) \tag{86}$$

4.4.5.1.1 Total harmonic distortion test method

To estimate the total harmonic distortion, use the sine wave test setup (Figure 3) with a test signal consisting of a pure, large amplitude sine wave at frequency f_i. Acquire K data records of M points each from the ADC under test at sample frequency f_s. Let $x_k[n]$ represent the kth record of sine-wave data for $k = 1,2,\ldots,K$. For each $x_k[n]$ record, compute the DFT, $X_k[f_m]$, $f_m = mf_s/M$, where m is an integer from 0 to $M-1$. The K sets of data are used to compute an averaged magnitude spectrum of the DFT bins at each basis frequency f_m in Equation (87).

$$X_{\mathrm{avm}}[f_m] = \frac{1}{K}\sum_{k=1}^{K}|X_k[f_m]|, \qquad m = 0,\ 1,\ 2,\ \ldots,\ M-1 \tag{87}$$

The averaged spectral magnitude, X_{avm}, is used because it has a smaller variance than the non-averaged spectral magnitude, X_k, as the standard deviation of the random errors in X_{avm} is less (by approximately $K^{-0.5}$) than it is for $|X_k|$.

Identify the set of frequencies, f_h, which corresponds to the chosen set of harmonics of the input test frequency. For a test tone at frequency f_i, the harmonics are aliased so that f_h lies between 0 and the sampling frequency f_s. Aliasing is accounted for by means of Equation (88), where 10 is the default value for H:

$$f_{h[n]} = (nf_r + Mf_s)\ \mathrm{MODULO}\ f_s, \qquad n = \pm\,[2,3,\ldots,H] \tag{88}$$

This procedure locates both Euler components of the aliased harmonics. Note that $f_{h[n]}$ is the aliased frequency of the nth harmonic of f_i. The (integer) index for the harmonic frequency is given by n_h as shown in Equation (89).

$$n_h = Mf_{h[n]}/f_s \tag{89}$$

The variable, n_h, is an integer only if the test frequency, f_i, coincides exactly with a DFT basis frequency, mf_s/M.

THD is generally function of both the amplitude, $X_{\mathrm{avm}}(f_i)$, and the frequency, f_i of the input sine wave. Thus, the amplitude and frequency of the input for which THD measurement(s) are made shall be specified.

4.4.5.1.2 Additional comments

The test described above is based on DFT analysis (e.g., via DFT) of non-windowed sample sets. It is therefore necessary to know accurately, or control, the test frequency, f_i, so that it coincides exactly with a DFT basis frequency. In addition, the test and sample frequencies should be selected as described in 4.1.4.3 such that all possible ADC states within the amplitude range of the test signal can be sampled.

It is possible to omit windowing only when the test signal frequency can be precisely set to a DFT basis frequency and the test and clock signal sources have sufficiently low phase noise. If the above frequency setting and purity conditions are not suitably established, the THD measurement accuracy will be compromised due to the spreading of the test signal energy across multiple DFT basis frequencies. Windowing is not recommended for these procedures due to the widening of resolution bandwidth.

4.4.5.2 Total spurious distortion

The total spurious distortion (TSD) is the rms value of the sum of the spurious components in the averaged spectral output of the ADC.

4.4.5.2.1 Total spurious distortion test method

To measure TSD, use the THD procedure (see 4.4.5.1.1), but replace the set of harmonic frequencies, $f_{h[n]}$, with the set of P spurious frequencies, $f_{sp[n]} = \{f_{sp1}, f_{sp2}, \ldots, f_{spP}\}$. Each of the spurious frequencies in f_{sp} is the frequency of a persistent spectral output component that is neither the fundamental nor a harmonic distortion component. The set is determined by inspection of the ADC output spectrum (see 4.4.5.1.1) and so there are no direct equations to determine this set of frequencies. Their indices are given by $n_{sp} = f_{sp}M/f_s$. The TSD is then estimated using the procedure developed for the THD measure. The set P shall be specified.

TSD is generally a function of both the amplitude, $X_{avm}(f_i)$, and the frequency, f_i, of the input sine wave, and also the ADC sample frequency f_s. Thus, the amplitude and frequency of the input, and the sample frequency, for which TSD measurement(s) are made shall be specified.

4.4.5.2.2 Comments

It should be noted that some ADCs are capable of producing extremely high-order harmonics (>100th) and care should be exercised to determine whether or not a spur in the spectrum is actually a harmonic. It is also true that whenever f_r is set on an odd numbered basis frequency of the DFT, then all spectral components of the DFT are actually harmonically related to f_r. The idea of spuriousness is then determined by selection of some arbitrary number for H beyond which all components are considered to be spurious rather than harmonic. This is tricky. The apparently high-order harmonics are either due to quantization error for the sampling of noise-free periodic signals or are sometimes found to be intermodulation products between f_r and $f_s/2$. Such hypotheses can be checked by changing f_i and noting how the candidate spur moves in the spectrum.

4.4.5.3 Spurious free dynamic range

For a pure sine wave input, the spurious free dynamic range (SFDR) is the ratio of the amplitude of the averaged DFT value at the fundamental frequency, f_i, to the amplitude of the averaged DFT value of the largest magnitude harmonic or spurious signal component observed over the full Nyquist band, $\max\{X_{avm}[f_h] \cup \{X_{avm}[f_{sp}]\}$, given in Equation (90).

$$\mathrm{SFDR}_{dB} = 20\log_{10}\left(\frac{|X_{avm}(f_r)|}{\max\limits_{f_{sp}\cap f_h}\left(\left|X_{avm}\left(f_{sp}\right)\right| \cup |X_{avm}(f_h)|\right)}\right) \tag{90}$$

SFDR is generally a function of both the amplitude, $X_{avm}(f_i)$, and the frequency, f_i, of the input sine wave, and possibly of the ADC sample frequency f_s as well as input noise or dither. Thus, the amplitude and frequency of the input, and the sample frequency, for which SFDR measurement(s) are made shall be specified.

4.4.5.3.1 Comments

The term *spurious free dynamic range* is often used for this measure where both harmonic distortion and spurious signals are considered to be undesirable *spurs* in the spectrum of a sampled pure sine wave. SFDR is used to indicate the ADC usable dynamic range beyond which special detection and threshold problems occur in spectral analysis.

4.4.6 Intermodulation distortion

Intermodulation distortion may occur whenever an ADC is sampling a signal composed of two or more sine waves or narrow-band signal groups. This subclause describes different measures

that are used to quantify such behavior. Intermodulation distortion spectral components may occur at sum and difference frequencies for all possible integer multiples of the input frequency tones or signal group frequencies. It is a phenomenon due to modulation and can be explained through the use of power series to model the nonlinear transfer function, or integral characteristic, of the device under test.

The measure described in the following subclause is based upon the use of an input composed of two independent pure sine waves. The cautionary comments given in 4.4.6.1.2 also apply to this test.

4.4.6.1 Two-tone intermodulation test method

Set the input test frequencies, f_{r1} and f_{r2}, at values that are an odd number of DFT bins away from $f_s/2$, with $f_{r2}>f_{r1}$. The difference, Δf, between f_{r2} and f_{r1} is then always an even number of DFT bins.

The spectrum of interest is the averaged magnitude spectrum, $X_{avm}[f_{imf}]$, as specified in Equation (87). Intermodulation distortion magnitudes for a two-tone input signal are found at specified sum and difference frequencies, f_{imf}, noted below in Equation (91) and Equation (92).

Difference frequencies:

$$f_{imf} = |(i)f_{r2} - (j)f_{r1}| \tag{91}$$

Sum frequencies:

$$f_{imf} = (i)f_{r2} + (j)f_{r1} \tag{92}$$

where $i, j = 0, 1, 2, 3, \ldots$ are integers, such that $|i| + |j| > 1$.

4.4.6.1.1 Comments on test procedure

There are no specific guidelines to specify which frequencies and signals should be used to perform intermodulation tests since the test parameters are influenced by each individual application. The size of Δf depends upon the application and the information desired.

The range for the integers i and j only need span nonnegative values; however, conjugate Euler frequencies can be determined using negative integers if desired. Range limits of three or four are appropriate for an ADC whose harmonic distortion test (see 4.4.5) shows that second and third harmonic distortion is dominant. Note that for small Δf, the intermodulation frequencies are clustered around harmonics of f_{r1} and f_{r2}. The location of the aliased intermodulation frequencies, within the sampling band, follows the modulo f_s procedure specified in 4.4.5.1.1 through Equation (88) and Equation (89).

Two-tone intermodulation distortion is generally a function of the amplitudes, $X_{avm}(f_{r1})$ and $X_{avm}(f_{r2})$, and the frequencies, f_{r1} and f_{r2}, of the input components. Thus, the amplitudes and frequencies of the input components for which intermodulation distortion measurement(s) are made shall be specified.

4.4.6.1.2 Additional comments

Note that the term "mth-order" is commonly used to describe specific nonlinear system behavior such as "third-order" intercept points, etc. The "mth-order intermodulation products" are found for those values of i and j that satisfy $m = |i| + |j|$, for the sum and difference frequencies defined by Equation (91) and Equation (92), e.g., for $m = 3$, $(i, j) = (3,0)$, $(2,1)$, $(1,2)$, and $(0,3)$. The frequencies found for $i = 0$ or $j = 0$ correspond to harmonic distortion. However, the measured distortion may be different than that measured for single sine wave input due to the presence of the other input sine wave.

A typical set of intermodulation distortion tests might involve three pairs of frequencies f_{r1} and f_{r2}, e.g., pairs of frequencies close to 0, $f_s/4$, and $f_s/2$, for a conventional Nyquist-band-limited ADC application. The three pairs of frequencies would be exercised at different input amplitude

combinations, e.g., each at −7 dB, −20 dB, and −40 dB below full scale (dBFS); or one tone could be held at −7 dBFS while the other is incremented in equal steps from the noise floor to −7 dBFS. Other ADC applications, such as intermediate-frequency (IF) sampling, may require intermodulation distortion tests with input frequencies spanning from $f_s/2$ to f_s; etc.

One caution about this test is that it is important that the test-input signal should be free of any significant amount of intermodulation distortion. This is not easy wherever a large ADC dynamic range (12-bits or greater) and wide bandwidths are involved. Intermodulation distortion can easily occur between two signal generators that have output-leveling circuitry and are coupled to one another through balanced, or so-called isolated, ports of a hybrid, and other coupling circuits. In addition, the hybrids, or passive filters, used to combine two tones should be operated well within their linear range limits in order to avoid the generation of intermodulation distortion in the resulting test signal input to the ADC.

4.4.6.2 Multi-tone intermodulation distortion

Multi-tone intermodulation distortion tests are often used to assist in the system design process to determine limits for signal dynamic range, useful frequency bands for different signal groups, and where to set the input signal noise floor so as to mask small intermodulation components for a given ADC. Single-tone harmonic distortion measures are useful to obtain general ideas about the linearity of a given ADC, but such data do not lead directly to models that predict useful intermodulation performance measures for independent input signal groups.

A typical test procedure uses a computer-controlled DAC to generate a signal composed of a set of sine waves having frequencies that are set at DFT bin center frequencies. Gaps between the tones are used as observation points to measure intermodulation distortion in the spectrum of X_{avm} as the amplitudes of the tones are uniformly increased from the noise floor to a level where the signal starts to be clipped as it exceeds the ADC full-scale range. Such a test provides results similar to the noise power ratio (NPR) test, but allows for better simulation of expected signal group waveforms. Since such tests are application specific, there are no useful equations provided here to describe this procedure or the quantification of its results.

4.5 Noise (total)

Noise is an ambiguous term. When the word *noise* is used without qualification (e.g., *random noise*, *quantization noise*) in this standard, it shall be assumed to refer to total noise. *Total noise* is any deviation between the output signal (converted to input units) and the input signal except for deviations caused by linear time-invariant system response (gain and phase shift), or a dc level shift. For example, noise includes the effects of random errors, fixed pattern errors, nonlinearities, and aperture uncertainty. Notable examples of such effects and deviations here defined as noise include quantization error, harmonic and intermodulation distortion, spurious distortion. This definition of total noise should be compared to the definition of random noise in 4.5.3.

SINAD is the same as the term SNR in IEEE Std 1057-1994. The term SNR is not used here because, in the context of ADC testing, it is used in different ways by different concerned parties and is thus too ambiguous. For instance, as of this writing, in the ADC industry, SNR often is equivalent to SNHR, the ratio of the signal to the portion of the noise that is not harmonic distortion.

4.5.1 Signal-to-noise and distortion ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio of the signal to the total noise. Unless otherwise specified, it is assumed to be the ratio of root-mean-square (rms) signal to rms noise,

including harmonic distortion, for sine wave input signals. SINAD depends on the amplitude and frequency of the applied sine wave.

4.5.1.1 SINAD test method

To estimate SINAD, apply a sine wave of specified frequency and amplitude to the ADC input. A large signal is preferred. The frequency of the input sine wave is called the fundamental frequency. Almost any error source in the sine wave input other than gain accuracy and dc offset can affect the test result. So, it is recommended that a sine wave source of good short-term stability be used and that the sine wave input be highly filtered to remove distortion and random noise from the input signal.

Take a record of data. Fit a sine wave to the record at the fundamental frequency as per 4.1.4. Compute the estimate of the rms value of the noise as shown in Equation (93).

$$\text{rms noise} = \left[\frac{1}{M}\sum_{n=1}^{M}(y_n - y'_n)^2\right]^{1/2} \tag{93}$$

where

y_n is the sample data set,

y'_n is the data set of the best-fit sine wave.

The signal-to-noise and distortion ratio (SINAD) is given by Equation (94)

$$\text{SINAD} = \frac{\text{rms signal}}{\text{rms noise}} \tag{94}$$

where

rms signal is equal to sine wave peak amplitude/$\sqrt{2}$.

4.5.1.2 SINAD test in the frequency domain

SINAD can be determined equivalently from the frequency domain as a consequence of Parseval's theorem. Follow test procedures as described in 4.5.1.1. SINAD is the ratio of the rms input signal to the rms noise and distortion (NAD). Both quantities can be determined from the DFT of data records, as was done for harmonic distortion in 4.4.5. The rms signal, A_{rms} (in LSBs), is obtained from Equation (85). Let E_{avm} equal the residual spectrum of X_{avm} [Equation (87)] after the bins at $f_{\text{m}} = 0$ (dc) and test frequencies, f_{i} and $(f_{\text{s}} - f_{\text{i}})$, have all been set to zero (excised from the spectrum). Then the rms noise is found from the sum of all the remaining Fourier components as shown in Equation (95).

$$\text{rms noise} = \frac{1}{M}\left[\sum_{m=0}^{M-1} E_{\text{avm}}(f_m)^2\right]^{1/2} \tag{95}$$

SINAD is then given by substitution of these measures into Equation (94).

4.5.1.3 SNHR from the frequency domain

The ratio of the signal to the portion of the noise that is not harmonic distortion, SNHR, is obtained from the DFT by excising the signal harmonic frequencies, $f_h[n]$, identified in Equation (86), from the test signal spectrum. The input rms signal, A_{rms} (in LSBs), is obtained from Equation (83). Then let N_{avm} equal the averaged DFT spectrum, X_{avm}, with the components (bins) at dc, the test frequencies f_{i} and $(f_{\text{s}} - f_{\text{i}})$, and the specified harmonic frequencies $f_h[n]$, all set to zero (excised). The rms noise is

then found from the sum of all the remaining Fourier components as shown in Equation (96).

$$\text{rms noise} = \frac{1}{M}\left[\sum_{m=0}^{M-1} N_{\text{avm}}(f_{\text{m}})^2\right]^{1/2} \tag{96}$$

SNHR is then given by substitution of these measures into Equation (94).

4.5.1.4 Comments on SINAD and SNHR

These ratios are both proportional to the test signal, A_{rms}, and it is customary to use a near full-scale signal for these measures. However, if clipping should occur, the measures will be severely degraded. In addition, these measures are generally a function of amplitude, $X_{\text{avm}}(f_{\text{i}})$, and the frequency, f_{i}, of the input sine wave. Thus, the amplitude and frequency of the input, for which the SINAD and/or SNHR measurements are made, shall be specified.

4.5.1.5 Normalized signal-to-noise measures

For a variety of ADC applications and comparative purposes, the use of a signal-to-noise ratio normalized to a 1 Hz bandwidth is often used. The measure is normally obtained from the ratio of signal to the portion of noise that is not harmonic distortion, as in the above SNHR measure, using a sinusoidal test signal. The ideal signal-to-noise ratio normalized to a reference bandwidth of 1 Hz is given by Equation (97).

$$\text{SNR}_{1\,\text{Hz}} = 10\log_{10}\left(\frac{\text{FSR}^2/8}{1(\text{Hz})(Q_{\text{eff}}^2/12\,B_0)z}\right)(\text{dB}) \tag{97}$$

where FSR (in LSBs) is the nominal full-scale range of the ADC, Q_{eff} is $(12)^{1/2}$ times the rms noise given by Equation (96), and B_0 is the Nyquist bandwidth (in Hz). When the normalized signal-to-noise ratio is determined over some other specified bandwidth, B, and test amplitude, A_{rms} as obtained from Equation (85), then a bandwidth signal-to-noise ratio (BWSNR) measure is defined as given by Equation (98), Equation (99), and Equation (100).

$$\text{BWSNR} = 10\log_{10}\left(\frac{A_{\text{rms}}^2}{B(Q_{\text{eff}}^2/12B_0)}\right) \tag{98}$$

$$\text{BWSNR} \equiv 10\log_{10}\left(\frac{\text{FSR}^2/8}{(1\,\text{Hz})(Q_{\text{eff}}^2/12B_0)} \times \frac{A_{\text{rms}}^2}{\text{FSR}^2/8} \times \frac{(1\,\text{Hz})}{B}\right) \tag{99}$$

$$\text{BWSNR} = \text{SNR}_{1\,\text{Hz}} + A_{\text{dBFS}} - B_{\text{dBHz}}(\text{dB}) \tag{100}$$

BWSNR is normally measured using a near full-scale sinusoid ($A_{\text{dBFS}} = -0.5$) at a near Nyquist bandwidth ($B_{\text{dBHz}} = 10\log_{10}(B/1\text{Hz})$). This parameter values exercise expected noise mechanisms such as slewing, digital ground noise, decimation rounding effects, etc.; and yield appropriate extrapolations for the 1 Hz normalized measure. The BWSNR notation is recommended for this near full-scale test. A small signal bandwidth signal-to-noise ratio (SSBWSNR) notation is recommended for those instances where it is desired to measure and specify a normalized ratio extrapolated from a small signal estimate of the signal-to-noise ratio. A measure determined in this manner can be in error by a few dB, and so the measure needs to be qualified.

Therefore, it is recommended to specify a small signal normalized measure, SSBWSNR, whenever a small amplitude (< -40 dBFS) is used. Equation (99) is used to define BWSNR for $A_{\text{rms}} > -40$ and

to define SSBWSNR for $A_{\text{rms}} < -40$. The extrapolated and normalized signal-to-noise ratio is then given by Equation (101).

$$\left.\begin{array}{ll} \text{SNR}_{1\text{Hz}} = \text{BWSNR} - A_{\text{dBFS}} + B_{\text{dBHz}} & \text{for } A_{\text{dBFS}} > -40 \\ \text{SNR}_{1\text{Hz}} = \text{SSBWSNR} - A_{\text{dBFS}} + B_{\text{dBHz}} & \text{for } A_{\text{dBFS}} < -40 \end{array}\right\} \tag{101}$$

4.5.2 Effective bits

For an input sine wave of specified frequency and amplitude, after correction for gain and offset, the effective number of bits (ENOB) is

$$\text{ENOB} = N - \log_2\left(\frac{\text{rms noise}}{\text{ideal rms quantization error}}\right) = \log_2\left(\frac{\text{full scale range}}{\text{rms noise} \cdot \sqrt{12}}\right) \tag{102}$$

where N is the number of digitized bits.

The second equality in Equation (102) comes from [see Equation (103)]

$$\text{ideal rms quantization error} = \frac{Q}{\sqrt{12}} \tag{103}$$

Effective bits generally depend on the amplitude and frequency of the applied sine wave. The amplitude and frequency at which the measurement was made shall be specified.

The effective bits method is one of comparing the amount of rms noise produced by the ADC under test to the rms quantization noise level of an ideal ADC having that amount of bits of resolution. In other words, if for a sine wave input of given frequency and amplitude, a real 10-bit ADC has an ENOB of 9.0, then it produces the same rms noise level for that input as an ideal 9-bit ADC would.

4.5.2.2 Comment on ideal quantization error

The input signal value corresponding to an ADC output code is best assumed to be the center of that code's bin. An input signal falling into a code bin not at the center generates quantization error amounting to the difference of the signal value from the center of the bin. To evaluate the typical size of the quantization error, its probability density function (PDF) must be determined. For large signal sine wave inputs, and ideal quantization (all code bin widths equal to the ideal width Q), the quantization error PDF is well approximated as a uniform distribution between $-Q/2$ and $+Q/2$. Thus the ideal quantization error rms is the standard deviation for that PDF, or $Q\sqrt{12}$.

4.5.2.3 Comment on relationship of effective bits and SINAD

SINAD and ENOB are related by Equation (104).

$$\text{ENOB} = \log_2(\text{SINAD}) - \frac{1}{2}\log_2(1.5) - \log_2\left(\frac{A}{(V/2)}\right) \tag{104}$$

or equivalently by Equation (105)

$$\text{SINAD} = \left(\sqrt{1.5}\right) \times \left(\frac{A}{V/2}\right) \times 2^{\text{ENOB}} \tag{105}$$

where

A is the amplitude of the sine wave fitted to the output,

V is the full-scale range of the ADC under test.

A different formulation of effective bits omits the third term of Equation (104). This formulation gives results for effective bits which differ from those in 4.5.2 in all cases other than for full-scale input test signals.

4.5.2.4 Comment on significance of record size

See 4.1.4.5.

4.5.2.5 Comment on effects of jitter or phase noise on sine wave tests

Time jitter (also called phase noise in the frequency domain) in the sine wave signal source produces both random and systematic errors for sine wave tests. A consequence of jitter (see Souders et al. [B40]) is that it spreads the energy of the original sine wave over a broad spectrum of frequencies, reducing the amplitude of the fundamental component (for $\sigma_t \ll 1/f$) approximately by the factor shown in Equation (106).

$$1 - \frac{\omega^2 \sigma_t^2}{2} \tag{106}$$

where

f is the signal frequency fundamental component, in Hz,

ω is equal to $2\pi f$,

σ_t is the standard deviation of the jitter, in seconds.

The energy lost in the fundamental component shows up as broadband noise that has an rms value (computed over a complete period of the input sine wave) given by Equation (107)

$$V_{\text{noise}} \approx V_{\text{p}} \frac{\omega\, \sigma_t}{\sqrt{2}} \tag{107}$$

where V_{p} is the sine wave peak amplitude.

The jitter-induced noise is distributed according to the time-derivative of the signal, approaching zero at the sine wave peaks, and reaching a maximum at the zero crossings given approximately by Equation (108).

$$\sigma_{\max} = \omega V_{\text{p}} \sigma_t \tag{108}$$

where $\sigma_{\max}$ is the maximum value of the standard deviation of the amplitude noise, occurring at the zero crossings.

If a sine fit is performed on the sampled sine wave with jitter, the amplitude of the estimated sine wave will be reduced by the factor given in Equation (106). Furthermore, if repeated acquisitions of the waveform are averaged, the result will be a sine wave with amplitude reduced by the same factor. Note that if the original sine wave were measured using a ''true rms'' responding instrument, e.g., an instrument that uses thermal transfer techniques, the measured value will NOT be reduced by this factor; this is because the total energy is not changed by jitter, it is only redistributed.

Jitter in the sine wave source limits the signal-to-noise ratio and the number of effective bits that can be measured. Substituting Equation (107) for rms noise in the effective bits formula [Equation (109)] gives

$$\text{ENOB} = \log_2 \left[\frac{\text{FSR}}{V_{\text{noise}} \times \sqrt{12}} \right] \tag{109}$$

and, for a large signal sine wave (i.e., $V_p \times$ FSR/2), this gives [Equation (110)]

$$\text{ENOB} = -0.7925 - \log_2\left[\frac{\omega\sigma_t}{\sqrt{2}}\right] = -0.2925 - \log_2 \omega\sigma_t \tag{110}$$

Table 3 gives the maximum effective bits that can be measured as a function of the jitter standard deviation, expressed as a fraction of the sine wave period.

Table 3—Maximum effective bits versus normalized jitter (fraction of sine wave period)

σ_t**f**	10^{-1}	10^{-2}	10^{-3}	10^{-4}	10^{-5}	10^{-6}
ENOB_{max}	0.4	3.7	7.0	10.3	13.7	17.0

It is unusual to find jitter specified for sine wave sources; instead, phase noise is more commonly specified. Unfortunately, it is not a simple task to compute jitter from typical phase noise specifications. An alternative approach is to measure the jitter directly. Wideband sampling oscilloscopes, e.g., often provide simple procedures for measuring signal jitter, with resolution that is usually adequate for most ADC applications.

4.5.2.6 Effects of harmonic distortion on sine wave tests

Harmonic distortion in the sine wave signal source can cause direct errors in measurements of SINAD, effective bits, and total harmonic distortion. In the worst case, the distortion of the ADC under test is dominated by a single harmonic component (frequency) of amplitude A_H, and the same harmonic component (and same phase) dominates the distortion of the signal source, with smaller amplitude, B_H. The true total harmonic distortion of the ADC is given by $20\log_{10}(A_H/A)$, where A is the amplitude of the fundamental component. On the other hand, the measured total harmonic distortion, assuming $B_H \ll A_H$, is given approximately by $20\log_{10}(A_H(1+B_H/A_H)/A)$. The difference between measured and true THD is given in Table 4 for several values of B_H/A_H. Similar results can be computed for SINAD and effective bits measurements, and example errors for these parameters are also included in Table 4.

Table 4—Worst-case degradation in measured performance

B_H/A_H	0.25	0.125	0.1	0.0625	0.05	units
SINAD	−1.94	−1.02	−0.83	−0.53	−0.42	dB
THD	1.94	1.02	0.83	0.53	0.42	dB
ENOB	−0.32	−0.17	−0.14	−0.09	−0.07	bits

More common but less serious cases occur when the distortion is spread out over many frequencies, and especially when the distortion in the signal source occurs at frequencies that are different from the major distortion frequencies of the ADC under test. In those cases the components combine orthogonally (i.e., root-sum-squares). In this case, if B_H is the amplitude of the major distortion component of the sine wave generator, and it is a different frequency from that of the major distortion component (with amplitude A_H) of the ADC, then the measured THD is given approximately by $20\log_{10}(A_H(1 + B_H^2/2A_H^2)/A)$. Table 5 reports errors in SINAD, THD, and ENOB that occur under these less serious conditions.

As a rule of thumb, a value of B_H/A_H of 0.1 (−20 dB) should be adequate for either case, and a value of 0.25 (−12 dB) should be adequate if the components are orthogonal. It is relatively easy to measure the distortion of a sine wave source using a spectrum analyzer, provided that the distortion in not

Table 5—Degradation in measured performance, assuming orthogonal components

B_H/A_H	0.25	0.125	0.1	0.0625	0.05	units
SINAD	−0.27	−0.07	−0.04	−0.02	−0.01	dB
THD	0.27	0.07	0.04	0.02	0.01	dB
ENOB	−0.04	−0.01	−0.01	−0.00	−0.00	bits

lower than −80 dB. If lower levels of distortion are required, then carefully designed notch filters should be used to reject the fundamental component, passing only the distortion components on to the spectrum analyzer. Care must be taken to account for any attenuation of the harmonic components caused by the filter. If the signal source does not have adequate spectral purity by itself, it can be improved with low pass or band pass filters. THD values of −80 dB can usually be achieved with relatively inexpensive commercial filters. To achieve significantly lower THD values usually requires specially designed filters (including the notch filters used for verification) constructed with linear, passive components; amplifiers and iron core inductors, e.g., often generate additional distortion that is difficult to remove.

4.5.3 Random noise

Random noise is a non-deterministic fluctuation in the output of an ADC, described by its frequency spectrum and its amplitude statistical properties. For the measurements in this clause, the following noise properties are assumed: the power spectrum is flat (white noise), and the amplitude probability density function is stationary.

4.5.3.1 Test method

Set up the ADC under test with a constant input signal source, of specified output impedance, having noise level at least four times less than the level of accuracy required for the ADC random noise measurement. Take two records of data M samples long, and subtract one from the other; the subtraction eliminates fixed-pattern errors. In Equation (111) the noise variance may be estimated from

$$\sigma^2 = \frac{1}{2M}\sum_{n=1}^{M}(y_{an}-y_{bn})^2 \tag{111}$$

where

σ^2 is the noise variance,

y_{an} and y_{bn} are the noise record samples,

M is the number of samples.

When the random noise standard deviation σ is measured here to be equal to or less than Q, use the method of 4.5.3.2 instead.

4.5.3.2 Alternative test method for low noise ADCs

Connect the output of a triangle wave generator to the signal input of the ADC. Adjust the output amplitude to about ten code transition levels peak-to-peak (see 4.5.3.3). Trigger the ADC on the beginning of the positive-going portion of the triangle. Adjust the frequency of the triangle wave generator such that one period of the triangle wave subtends one record length. The record length should be commensurate with the desired measurement accuracy (see 4.5.3.3). Capture two records,

and find their difference as given above in 4.5.3.1. Use Equation (112) and Equation (113) to get the noise variance σ^2:

$$\text{mse} = \frac{1}{M}\sum_{n=1}^{M}(y_{an} - y_{bn})^2 \tag{112}$$

$$\sigma^2 = \left[\left(\frac{\text{mse}}{2}\right)^{-2} + \left(\frac{0.886\ \text{mse}}{Q}\right)^{-4}\right]^{(-1/2)} \tag{113}$$

where

mse is the mean square error,

σ^2 is the noise variance,

y_{an} and y_{bn} are the noise record samples,

M is the number of samples.

Note that as the random noise increases, Equation (113) converges to Equation (111).

4.5.3.2.1 Note on amplitude of triangle wave used for test

The triangle wave provides a means of slowly slewing the ADC over multiple code transitions at a relatively constant rate. The subtraction process removes the contribution of the triangle wave to the result to the extent that the two repetitions are identical. Any differences due to noise, jitter, etc. will contribute to the apparent result. Consequently, unless the output of the generator can be independently judged to have a sufficiently low noise level, it is best to keep the amplitude low. This means that only a part of the full-scale range of the ADC can be explored with each measurement.

4.5.3.2.2 Note on desired accuracy

The standard deviation of an estimate of random noise standard deviation is given by

$$\sigma_\sigma = \frac{\sigma}{\sqrt{M-1}} \tag{114}$$

where

σ_σ is the standard deviation of the estimate of random noise amplitude,

σ is the random noise standard deviation,

M is the number of independent random noise samples.

4.5.3.3 Alternative random noise and hysteresis test method based on a feedback loop

An alternative method for measuring random noise, hysteresis, and alternation bands employs the feedback loop method shown in Figure 8a and Figure 8b. The method often becomes impractical when conversion times are significantly longer than 10 μs. The feedback loop technique is shown in the figures for converters with voltage inputs. The method is easily extended to converters with other forms of input. The parameters N_1 and N_2 are used to define the magnitude of the change of the DAC input if the ADC output, k, is less than or greater than or equal to the code "k_{in}". The clock signals "Trig" and "Trig1" can generally be identical to each other.

This test method can determine the parameters of the random noise at a given code transition level of the ADC under test. The feedback loop works to find the transition level $T[k_{\text{in}}]$ at the lower edge

of the code bin whose code is the reference code value "k_{in}". The stable dc source is set to a value near the value which corresponds to that code. The stable source must have a noise level that is significantly less than that expected from the ADC under test. If $N_1 = N_2 = N$, and the change in the DAC output generated by a change in input code of N, is less than the standard deviation of the random noise being measured, then the voltage at the ADC input will adjust itself to a value which will cause the ADC output code to be greater than k_{in} 50% of the time.

Changing the ratio of N_1 to N_2 will force a change in the duty cycle of the codes being produced by the ADC under test. Table 6 illustrates how the average DAC output voltage is affected by a change in the ratio N_1/N_2. The tabulated values assume that the equivalent noise at the input to the ADC under test is Gaussian, with an rms value of σ.

A typical measurement sequence would involve calculating the average DAC output twice. The first time, the ratio N_1/N_2 would be set to 2.0. The second time the ratio would be set to 0.5. From Table 6 we see that the difference of the two measurements will be $2\times0.431\sigma$. The value of σ can be evaluated by dividing the difference in the voltage readings by 0.862.

Table 6—ADC input versus N_1/N_2 for alternate noise measurement method

N_1/N_2	ADC_{INPUT}	N_1/N_2	ADC_{INPUT}	N_1/N_2	ADC_{INPUT}
1.0	x	5.0	$x-0.967\sigma$	0.5	$x+0.431\sigma$
2.0	$x-0.431\sigma$	10.0	$x-1.335\sigma$	0.3333	$x+0.674\sigma$
3.0	$x-0.674\sigma$	15.0	$x-1.534\sigma$	0.25	$x+0.841\sigma$
4.0	$x-0.841\sigma$	20.0	$x-1.668\sigma$	0.2	$x+0.967\sigma$

The circuits whose block diagrams are shown in Figure 8 can be used for evaluating the size of the hysteresis or the alternation band. The spectral content of the ADC input is measured while $N_1 = N_2 = N$. The spectrum can be measured by performing a windowed Fourier analysis of the record recorded in the test sequence described in 4.1.2. A spectrum analyzer can be used to monitor the ADC input. If the ADC is ideal, there will be no obvious frequency lines noted at less than f_s. If an alternation band is present there will be a significant component at $f_s/2$. If hysteresis is present there will be a lower frequency component generated by a ramp spanning the hysteresis band. Hysteresis or alternation will become apparent only if the noise of the converter is smaller than the hysteresis or the alternation band.

4.5.4 (Random) noise power ratio

The dynamic performance of an ADC with broad bandwidth input is sometimes characterized by measuring a quantity known as the noise power ratio (NPR). In ADC applications where the input signal contains a large number of incoherent tones or narrow bandwidth signals, it is generally desired that distortion, due to combinations of strong signal components, should not interfere with detection of weaker signal components. An example of such an input signal is one which contains a large number of frequency-division multiplexed (FDM) voice channels. Since it is impossible to design a test that embodies the specific features of all possible applications, NPR has been adopted as a figure of merit for characterizing ADC performance in response to broad bandwidth signals. As explained below, the test leads to a number, the maximum NPR, by comparison of measured data to an ideal curve.

Analog-to-digital converters possessing measured noise power ratios that closely match theoretical NPR, for an ideal N-bit device, are desirable candidates for broadband signal applications, e.g., a signal containing many FDM channels.

Using a notch-filtered broadband white-noise generator as the input to the ADC under test, the noise power ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the DFT spectrum of the ADC output sample set.

4.5.4.1 NPR test method

Use the arbitrary waveform test setup (Figure 4). The normal procedure is to create a curve in a series of steps which proceeds as follows. A random noise process is generated such that it possesses an approximately uniform spectrum up to a chosen cutoff frequency, f_{co}, which is less than half the sampling frequency. A narrow band of frequencies is then removed from the noise using a notch filter. To obtain a meaningful measurement, the depth of the notch must be at least 10 dB greater than the NPR value being measured. In addition, the width of the notch should be narrow compared to the overall noise bandwidth. With the notched noise applied to the ADC input, the frequency spectrum of a captured code sequence is computed. See Figure 12a for an example spectrum. The NPR is then calculated as the ratio of the average power spectral density outside the notched frequency band, P_{No}, to that inside the notched band, P_{Ni}. This ratio is typically expressed in decibels [See Equation (115)].

$$\mathrm{NPR} = 10\log_{10}|P_{No}/P_{Ni}|\mathrm{dB} \tag{115}$$

Table 7 lists theoretical maximum NPR (NPR_{max}) values for ideal n-bit quantizers for both Gaussian and uniform random sources. These values were obtained from Equation (116) and Equation (117).

Table 7—Maximum NPR for Gaussian and uniform noise sources

Source	Uniform	Gaussian		
No. of bits	α (dB)	NPR_{max} (dB)	$+\alpha$ (dB)	NPR_{max} (dB)
6	−4.65	36.20	−10.31	29.94
8	−4.77	48.16	−11.87	40.60
10	−4.77	60.21	−13.04	51.56
12	−4.77	72.25	−14.02	62.71
14	−4.77	84.29	−14.80	74.01
16	−4.77	96.33	−15.45	85.40
18	−4.77	108.37	−16.04	96.88
20	−4.77	120.41	−16.62	108.41

4.5.4.2 NPR testing issues

Some experimentation with the following test procedures may be necessary to obtain reliable measures of the NPR.

4.5.4.2.1 Input signal filtering

In practice, it is usually necessary to lowpass filter the input noise signal to prevent aliasing and to obtain a uniform noise power across the input signal spectrum. When the noise bandwidth is lowpass filtered to obtain a bandwidth less than the Nyquist frequency, the peak data listed in Table 7 are valid for the Gaussian input signal since they are dependent upon the average input power. However, for the uniformly distributed input, the data deteriorate toward the Gaussian values since, as the signal is lowpass filtered, the convolution of signal with filter response converges toward a Gaussian process as the bandwidth is lowered from the full Nyquist band. If one plots NPR measurements based upon the input prior to lowpass filtering, then the input at maximum NPR will shift according to the bandwidth ratio, in decibels, of the filter cutoff frequency, f_{co}, to the Nyquist frequency, $f_s/2$.

4.5.4.2.2 Notch filter width

Another factor that affects measured NPR is the width of the notch filter. Assuming that the measured NPR is obtained from DFT spectral estimates, widening of the notch filter and averaging the noise power contained in the DFT bins inside the notch improves the estimated NPR in comparison with using a single bin for the estimate of average noise power in the notch. Making the notch too wide, however, degrades the estimated NPR since the assumption of a uniform noise spectrum could be jeopardized.

4.5.4.2.3 Windowing

For some cases, the depth of the filtered notch may be degraded due to spectral leakage. The use of windowing eliminates this effect at the expense of a small change in the noise floor. See 4.1.5 for additional details on the effects of windowing.

4.5.4.3 Measured and theoretical NPR

It is customary to plot measured and theoretical NPR versus the mean noise power of the input noise process (see Daboczi [B9]). For a non-ideal N-bit ADC, measured NPR curves follow theoretical response at small input power levels given that the ADC does not have excess internal noise. Measured NPR curves normally depart from theory prior to reaching theoretical maximum NPR due to ADC-generated harmonic and intermodulation distortions. It is also true that the measured curve will depart from theory for very small power levels where peak-to-peak signals are less than a least significant bit (LSB) of the ADC.

The maximum measured NPR value is used to specify ADC response to broadband signals with a single number but it is also necessary to specify the type of noise source used for the test.

The theoretical NPR equations for Gaussian and uniform distribution signals are given in Equation (116) and Equation (117) respectively (Irons et al. [B17]).

$$\mathrm{NPR_G} = \frac{\alpha^2}{\left[\frac{2^{-2N}}{3} - \frac{2\alpha}{\sqrt{2\pi}} e^{(1/2\alpha^2)} + (1+\alpha^2)\frac{2}{\sqrt{\pi}} \int_{1/\sqrt{2}\alpha}^{\infty} e^{-v^2}\, \mathrm{d}v\right]} \tag{116}$$

$$\mathrm{NPR_U} = \frac{(\sqrt{3}\alpha)^3}{\left[(\sqrt{3}\alpha)\, 2^{-2N} + (\sqrt{3}\alpha - 1)^3\, u(\sqrt{3}\alpha - 1)\right]} \tag{117}$$

where

α is equal to 2 $(V_{\mathrm{in}})_{\mathrm{rms}}$/ FSR,

N is the number of ADC bits,

u is the unit step function,

v is the dummy integration variable.

$(V_{\mathrm{in}})_{\mathrm{rms}}$ is the rms of the actual input to the ADC. Example plots of Equation (116) and Equation (117) compared with simulated measured data are shown in Figure 11a and Figure 11b for an 8-bit quantizer. An example simulated broadband signal for a 12-bit DAC-generated notch-filtered uniform distribution spectrum is shown in Figure 12a. The plot has several features that should be noted as follows: it is symmetric about its center, $f_s/2$; the middle notch is an anti-aliasing filter with cutoff f_{co}; and the left notch is the NPR measuring filter. The corresponding histogram for a 16K-sample set is

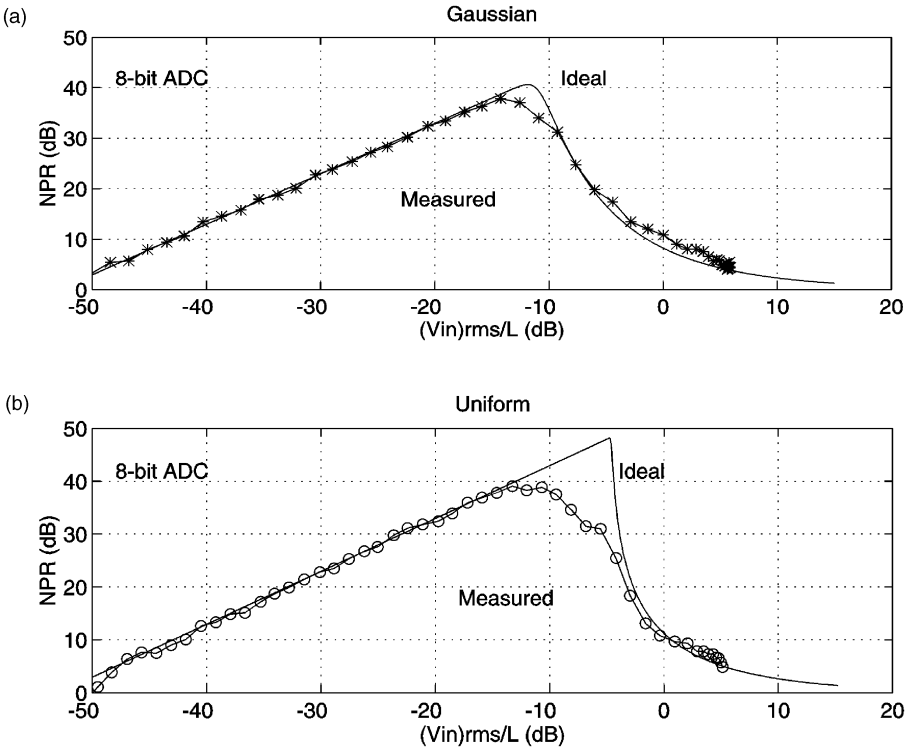

**Figure 11—(a) Plot of NPR from Equation (116);
(b) Plot of NPR from Equation (117)**

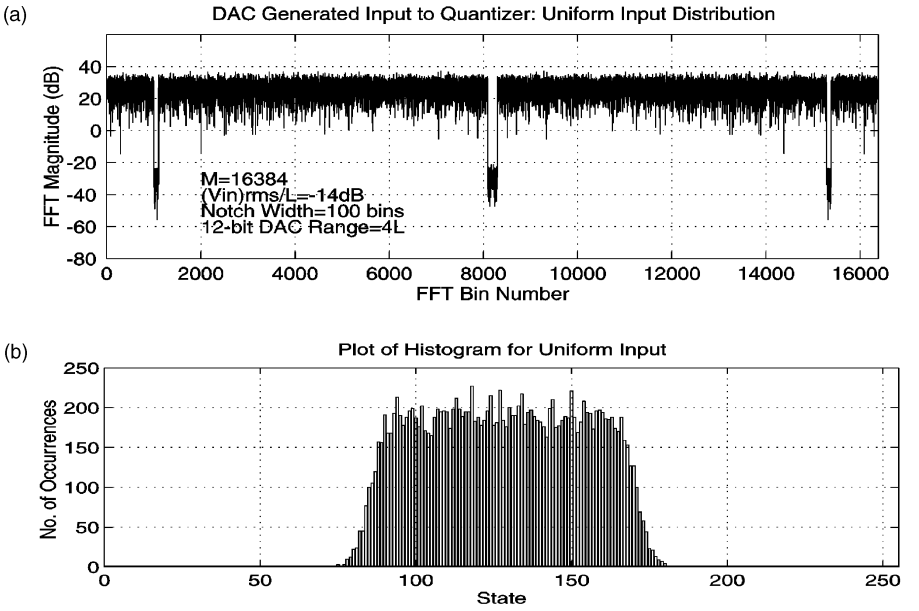

**Figure 12—(a) DAC-generated input to quantizer;
(b) Histogram from 16K-sample set**

shown in Figure 12b. Note that this histogram looks nearly uniform, but the rounding is due to spectral convolution with the anti-aliasing and notch filters.

4.5.4.4 Comments on NPR

Insight into the NPR response can be obtained by considering an ideal N-bit ADC. The mean-squared quantization error for such a device is $Q^2/12$. Assuming that the input signal does not saturate the ADC, the quantization error is independent of the input power level. This ideal quantization noise exhibits a uniform spectrum with the noise power evenly distributed over the full Nyquist band. When the input noise power is greater than the quantization power, an increase of 1 dB in input power yields a 1 dB increase in NPR, since the quantization power spectral density in the notch remains constant. The linear slope of the NPR curve is thus maintained as long as the ADC operates within its unsaturated signal range and other nonlinearities are not present in the ADC's response to the broadband test signal.

4.6 Step response parameters

The step response is the recorded response of the ADC under test to a perfect step input signal with designated baseline and topline.

4.6.1 Test method for acquiring an estimate of the step response

Use the step signal test setup (Figure 5). Use a suitable input step signal generator: in lieu of a perfect step, a suitable input step signal is one that has transition duration, overshoot, and settling time no greater than one-fourth of those expected from the ADC under test. Using this 4:1 performance ratio as a guideline, one should expect approximately a 3% error in the transition duration estimate. For overshoot and settling time, the uncertainty in the input step parameters will add equal uncertainty in the corresponding estimated ADC quantities. If smaller uncertainties are required, then deconvolution techniques may be applied to remove the input step signal imperfection (Daboczi [B9]).

If possible, before and after acquiring the actual step response data, determine the (static) initial and final values of the step, which are respectively the baseline and topline or the topline and baseline. If the pre-acquisition measurements of the initial and final values differ significantly from the post-acquisition measurements of the initial and final values (due to system drift during the data acquisition), estimate the initial and final values of the step as the average of their respective pre- and post-acquisition measurements. Acquire a record or records of samples of the ADC step response that are sufficiently long to include all features of interest, e.g., precursors, and electrical and thermal settling. In order to produce high resolution sampling of step response features and reduce errors due to aliasing, it may be necessary to use the method of equivalent-time sampling, as described in 4.1.3. To reduce the effects of random noise and aperture uncertainty, it is recommended that multiple records of the step response be ensemble averaged.

Significant error sources in acquiring the step response estimate include aliasing, jitter, random noise, ADC nonlinearities (such as slew rate limiting), input step imperfections, and inaccuracies or imprecisions of the frequencies used to control the ADC and the step generator during equivalent-time sampling (see Souders and Flach [B37] for more information).

The following subclauses describe how to determine ADC parameters from measured step response data. The initial and final values of the applied input step signal should be specified in the test results.

4.6.1.1 Comment on test results

On some ADCs, typically those that do not employ sharp cutoff anti-aliasing filters, the step response can be nonlinear when the slew rate approaches the slew rate limit (4.6.2). The value of this slew rate limit is dependent upon the ADC under test. The degree of resulting nonlinearity of the step response

increases with the steepness of the applied step. Because of this nonlinearity, the measured step response of such an ADC can be misleading. To eliminate the gross nonlinearities, the slew rate of the applied input step must be sufficiently below the slew rate limit. The statement of results should include the transition duration and amplitude of the applied step.

4.6.2 Slew rate limit

The slew rate limit is the value of output transition rate of change for which increased amplitude input step causes no change.

4.6.2.1 Test method

Record the step response (see 4.6.1) for an input step having an amplitude 10% of full scale. Determine and store the maximum rate of change of the output transition. Repeat this process, increasing the amplitude of the input step each time. When the maximum rate of change ceases to increase with increasing step amplitude, slew limiting is taking place and the slew rate limit is the largest recorded value for the maximum rate of change.

4.6.3 Settling time parameters

4.6.3.1 Settling time

Measured from the 50% point of the output transition, the settling time is the time at which the step response enters and subsequently remains within a specified error band around the final value. The final value is defined to occur 1 s after the beginning of the step.

4.6.3.2 Short-term settling time

Measured from the first mesial point (50%) of the output, the short-term settling time is the time at which the step response enters and subsequently remains within a specified error band around the final value. The final value is defined to occur at a specified time less than 1 s after the beginning of the step.

4.6.3.3 Long-term settling error

The long-term settling error is the maximum absolute difference between the final value specified for short-term settling time and the value 1 s after the beginning of the step, expressed as a percentage of the step amplitude.

4.6.3.4 Test method for settling time and short-term settling time

Record the step response (as per 4.6.1) to an input step using a record length sufficient to represent the step over the duration specified, or for at least 1 s when the duration is not specified. Two or more overlapping records with different sample rates may be required to achieve the necessary time resolution and the required duration. To reduce noise or quantization errors, it may be desirable to digitally filter the step response data before computing settling time parameters. For example, apply a moving average filter of the form as shown in Equation (118).

$$y_n = \frac{1}{(2r+1)} \sum_{s=-r}^{r} x_{n-s} \tag{118}$$

where

x_{n-s} is the value of the $(n-s)$th data point of the unfiltered step response,

y_n is the value of the nth data point of the filtered step response,

r is an integer defining the width of the moving average window.

If such a filter is used, the width of its window, $(2r+1)$, shall be specified in the test results.

Determine the time of occurrence of the first 50% point on the transition of the recorded waveform. Counting from that time, the settling time (or the short-term settling time) is the time at which the output waveform last enters the bound given by $V(t) \pm e$, where $V(t)$ is the value at the end of the specified duration and e is the specified error. When the duration is not specified, $V(t)$ is the value 1 s after the beginning of the step.

To measure the long-term settling error, record the same step used to determine the short-term settling time, with a record that spans at least a 1 s interval from the beginning of the step. The long-term settling error is the absolute difference between the value 1 s after the beginning of the step and the value at the end of the specified duration following the step, expressed as a percentage of the step amplitude.

4.6.3.5 Comment on settling time

The term settling time refers to the time required to settle to the steady state, dc value, to within the given tolerance. The dc value is assumed to be the value after a constant input has been applied for at least 1 s. Changes that occur after 1 s are considered drift, and may be due to room temperature fluctuations, component aging, and similar effects.

The term short-term settling time refers to the time required to settle to a relative value (perhaps different from the steady-state value), defined as the value at the end of a specified duration, for record lengths less than 1 s. If static offset, gain, and linearity corrections are used to assign true values to short-term settling data, the results will have an uncertainty given by the long- term settling error. The uncertainty results because of longer term settling phenomena, such as thermal imbalances that may occur after the short-term duration is complete, but which affect a steady-state measurement.

Note that only short-term settling time can be specified for ac-coupled ADCs.

4.6.4 Transition duration of step response

The transition duration of the step response is the duration between the 10% point and the 90% point on the recorded output response transition, for an ideal input step with designated baseline and topline. The algorithm used to determine the baseline and topline of the output step must be defined. The methods of IEC 60469-2 (1987-12) are preferred.

4.6.4.1 Test method

Record the step response (see 4.6.1) and determine the 10% and 90% points of the output transition using methods in IEC 60469-2 (1987-12). Linear interpolation is used to determine the 10% and 90% points when insufficient data points are available on the transition. The transition duration of the step response is the time between the first 10% point and the last 90% point on the transition.

4.6.5 Overshoot and precursors

Overshoot is the maximum amount by which the step response exceeds the topline, and is specified as a percent of the (recorded) pulse amplitude. Precursors are any deviations from the baseline prior to the pulse transition. They are specified in terms of their maximum amplitude as a percent of the pulse amplitude.

4.6.5.1 Test method

Record the step response (see 4.6.1). Determine the maximum overshoot by following the method in IEC 60469-2 (1987-12).

4.7 Frequency response parameters

4.7.1 Bandwidth (BW)

The ADC's bandwidth is the width of the passband of its frequency response. Specifically, it is the difference between the upper and lower −3 dB frequencies, which are the frequencies at which the gain of the ADC is −3 dB of the gain at a specified reference frequency within the passband. The reference frequency is typically chosen as a frequency where the gain is at or near its peak value in the passband. Many ADCs have no lower −3 dB frequency because their passbands extend down to zero frequency (dc); in such cases, their bandwidths are simply the values of their upper −3 dB frequency. In such cases, the reference frequency is often chosen to be zero, so that the reference gain is the dc gain. If a lower −3 dB frequency does exist, the upper and lower −3 dB frequencies should be specified in the test results along with the bandwidth, instead of the bandwidth alone, which is their difference.

The determination of the large signal upper −3 dB frequency can be nontrivial if an ADC starts to exhibit slew rate-induced nonlinearities below or near this frequency. It is recommended that an alternate figure of merit, useful power bandwidth, be used to describe such ADCs, as determined in 4.7.1.3. Linear system theory no longer applies to devices at these slew rates, and an upper −3 dB frequency, if it could be uniquely identified, would not be useful in the usual manner.

Below are two methods of determining bandwidth and methods for determining the useful power bandwidth. The first method uses sine-wave inputs, and can be done very quickly if the reference frequency and the approximate limit frequencies are known. The disadvantage of this method is the typically low accuracy of estimates of the analog input amplitudes, which reduces the accuracy of the bandwidth result as well. The second method uses the frequency response as determined by the DFT of the derivative of the step response, from 4.7.3. Its disadvantages are high noise at higher frequencies, and aliasing and first-differencing errors resulting from the frequency response estimation. The results of using the step response method are invalid in the presence of slew rate induced errors; this method is generally more useful for ADCs which contain analog bandwidth limiting circuitry before the quantizer(s). Converters prone to slew rate induced errors should specify useful power bandwidth and use the third method below.

Bandwidth may be measured at any stated signal amplitude and sampling rate. When the sampling rate is not specified, bandwidth is measured at the maximum sampling rate.

4.7.1.1 Bandwidth test method

This method uses sine waves of known frequencies and amplitudes to determine bandwidth. A large signal (3.1) sine wave is used, unless the small-signal bandwidth is to be determined. When small-signal bandwidth is to be determined, the peak-to-peak input amplitude used is less than 1/10 of full scale. Use the sine wave test setup (see 4.1.1.1). The input sine wave source should produce sinusoids of high spectral purity, harmonic distortion lower than that of the ADC under test, and should have stable output during the measurement time. The tested input frequencies should not be sub-harmonics of the ADC sampling rate; such frequencies can produce incorrect answers in this test.

Select an input reference frequency at which the ADC dynamic gain is at or near its peak value in the passband. The reference frequency should be stated with the test results. Connect the sine generator to the ADC input, set its frequency to the reference frequency, and acquire a sufficient number of data

records from the ADC output to determine the maximum peak-to-peak range of the signal, using a three-parameter or four-parameter sinefit (see 4.1.4). Using an ac voltmeter or other means, measure the amplitude of the applied input sinusoid at the same reference plane as that represented by the ADC input port. This input amplitude measurement must be done with care if high accuracy is required (see Kinard and Ti-Xiong [B23], Laug et al. [B25]). If the measured input amplitude parameter is the rms amplitude, A_{rms}, it must be converted to peak-to-peak amplitude, $A_{\text{p.–p.}}$, using Equation (119).

$$A_{\text{p.–p.}} = A_{\text{rms}} \times \sqrt{2} \tag{119}$$

Divide the peak-to-peak ADC output amplitude by the measured peak-to-peak input amplitude to determine the reference gain.

If the chosen reference frequency is zero, the reference gain is the static gain, as determined in 4.3. Alternatively to using the static gain as determined in 4.3, use a precision dc signal source to provide a constant input signal. Approximate the dc gain by the constant output signal level minus the measured static dc offset (see 4.3.1), divided by the input dc level.

Once the reference gain is determined, change the input frequency to another value that is not a sampling-rate sub-harmonic. Measure the maximum peak-to-peak range of the recorded data, and divide it by the measured input amplitude to find the gain at this frequency. Repeat this as necessary to find the upper (and, if it exists, lower) frequency closest to the reference frequency, at which the gain is 3 dB below the reference gain. If no lower −3 dB frequency exists, the upper −3 dB frequency is the bandwidth. If a lower −3 dB frequency exists, the difference between the upper and lower −3 dB frequencies is the bandwidth of the ADC.

4.7.1.2 Alternative bandwidth test method using time domain techniques

This method is used to determine the ADC bandwidth via the ADC frequency response determined in 4.7.3.1. It is desirable to have as many samples in the record as possible, to increase the resolution with which the bandwidth can be resolved from the DFT of the derivative of the step response. The sampling rate, or equivalent-time sampling rate, should be high enough to make aliasing errors negligible (see 4.7.3.2).

Choose the reference frequency f_{ref} from the DFT bins $f_k = k/(MT\text{s})$: choose the one within the passband such that the dynamic gain is at or near the peak gain of the passband. The reference frequency should be stated. Next, search the DFT bins to find the upper and, if applicable, the lower frequency samples closest to the reference frequency, at which the gain is 3 dB below the reference gain. The bandwidth is the difference between these upper and lower −3 dB sample frequencies (or, if a lower −3 dB frequency does not exist, the bandwidth is simply the upper −3 dB frequency value). To improve the bandwidth estimate, interpolate between the frequency samples above and below −3 dB in amplitude, to better estimate the actual −3 dB frequency.

4.7.1.3 Useful power bandwidth test method

The useful power bandwidth of a device is the large signal analog input frequency at which a record of the ADC's output data will be degraded by less than a specified amount. The type of degradation used to denote the useful bandwidth is dependent upon the architecture of the ADC and should be chosen on the basis of the type of slew rate degradation which the ADC typically exhibits. ADCs whose architecture begins to show spurious sparkle codes at high slew rates should use the frequency at which these sparkle codes begin to appear, to a specified confidence level. ADCs that begin to start missing codes should specify either a no-missing-codes power bandwidth or an equivalent metric such as SNHR greater than a specified number of dB. A compromise measure of degradation, SINAD greater than a specified number of dB, is most useful with ADCs that simultaneously show small-amplitude spurious sparkle codes and missing codes.

To test for useful power bandwidth at a stated frequency when a converter exhibits spurious sparkle codes, apply a large signal (90% of full-scale range or greater) sine wave at the frequency using the test setup of 4.1.1.1. Perform repeated SINAD tests, using the methods of 4.5.1.1 or 4.5.1.2 and storing the results of each test. The number of tests to perform is governed by both the number of samples used in each test and the desired confidence level of the results. The set of test results is then subjected to a statistical test for uniformity: the variance of the test results is computed and compared to a limit. ADCs exhibiting spurious sparkle codes in one to a few of the SINAD tests will result in a variance which is larger than the limit, while ADCs exhibiting no sparkle codes will show test result variance below the limit. While ADCs always exhibiting the sparkle codes will also meet the variance limit comparison, a simultaneous limit on the value of the test result will ensure that such devices are detected. Optionally, ADCs failing the variance comparison or the test value limit can be retested at a lower applied input frequency to see whether they meet a new, lower frequency, useful power bandwidth test.

To test for useful power bandwidth at a stated frequency when a converter exhibits missing codes, apply a large signal sine wave at the frequency to be tested, using the test setup of 4.1.1.1. Perform an SNHR test using the methods of 4.5.1.3, and compare the test result to the stated limit.

To test for useful power bandwidth at a stated frequency when a converter exhibits missing codes and/or small amplitude spurious sparkle codes, apply a large signal sine wave at the frequency to be tested using the test setup of 4.1.1.1. Perform a SINAD test using the methods of 4.5.1.1 or 4.5.1.2, and compare the test result to the stated limit.

While it is possible in each of the above tests to decrease/increase the input test frequency until the test passes/fails, and to thus determine the actual useful power bandwidth of each device, it is often more economical to pick a single, conservative test frequency and to test that all ADCs exhibit a useable power bandwidth greater than this minimum. ADCs tested in such a manner should state the input frequency used in the test and specify this frequency as the minimum useful power bandwidth.

4.7.2 Gain error (gain flatness)

Gain error, also known as gain flatness, is the difference between the dynamic gain, $G(f)$, of the ADC at a given frequency and its gain at a specified reference frequency, divided by its gain at the reference frequency. The dynamic gain of the ADC under test at a frequency f is the magnitude of the frequency response at that frequency. The reference frequency is chosen to be a frequency whose gain is at or near the peak gain of the ADC passband; typically it is the same frequency as the one used in the bandwidth test (see 4.7.1). For dc-coupled ADCs, the reference frequency is typically dc ($f = 0$). To determine gain error, first determine the dynamic gain. This may be done by using the sine-wave-based methods of 4.7.1 or from the differentiated step response method of 4.7.3. The gain error at frequency f is shown in Equation (120).

$$E_{\mathrm{G}}(f) = \frac{G(f) - G(f_{\mathrm{ref}})}{G(f_{\mathrm{ref}})} \times 100\% \tag{120}$$

where f_{ref} is the chosen reference frequency.

4.7.3 Frequency response and gain from step response

The frequency response of an ADC is its complex response (magnitude and phase) versus frequency. It is also the Fourier transform of its impulse response. The preferred method of presentation is in the form of plots of magnitude (gain) and phase versus frequency.

4.7.3.1 Frequency response and dynamic gain test method

Record the step response of the ADC under test (see 4.6.1), using the step signal test setup in Figure 5, an appropriate step signal, $s(t)$, and equivalent-time sampling if necessary (see 4.1.3). Determine to sufficient accuracy the step signal's input amplitude, s_0 (the magnitude of the difference between the step's input baseline and input topline). Select the ADC's (equivalent-time) sampling rate, T_s, high enough to give negligible aliasing errors based on the ADC bandwidth (see 4.7.3.2; if the bandwidth is unknown prior to this test, the test may have to be repeated, once the bandwidth is known, at a sufficient sample rate to make the aliasing errors negligible). Acquire a record of M samples of the step signal, with an epoch (MT_s) long enough to ensure that the topline of the step has settled to within the desired accuracy. Estimate the ADC's discrete-time impulse response, $h[n]$, by taking the discrete derivative of the step response samples, $s[n]$, in units of the output quantity, and dividing it by the step's input amplitude, s_0, in units of the input quantity. The discrete derivative is often estimated by the first difference of the samples in the record (Souders and Flach [B37]) as shown in Equation (121).

$$h[n] = \frac{1}{s_0} \times \frac{\mathrm{d}(s(n\,T_s))}{\mathrm{d}t} \cong \left\{ \begin{array}{ll} \left(\dfrac{s[n+1] - s[n]}{s_0 \times T_s} \right) & \text{for } n = 0, 1, 2, \ldots, M-2, \\ \left(\dfrac{s[n] - s[n-1]}{s_0 \times T_s} \right) & \text{for } n = M-1 \end{array} \right\} \tag{121}$$

Calculate the DFT of the impulse response using a non-weighted (rectangular) window. Multiply the result by the value of the sampling period, T_s. The result is an estimate, $H(f_k)$, of the frequency response of the converter, at the frequencies $f_k = k/(MT_s)$ given in Equation (122).

$$H(f_k) = T_s \times \sum_{n=0}^{M-1} h[n] \times \exp(-j2\pi kn/M), \quad k = 0, 1, 2, \ldots, (M/2) \tag{122}$$

Note that the frequency response is estimated only at discrete frequencies f_k. To estimate the frequency response at other frequencies, linearly interpolate between the closest discrete frequencies.

For most Fourier transform calculations, the phase spectrum typically is *wrapped*, that is, its values are modulo (2π); in other words, only the remainder after dividing by 2π is given. The wrapping is partly due to the delay between the start of the record and the position in the record of the step transition. This delay introduces a phase term that is linearly related to frequency. The delay, and the *linear phase* term it induces, are usually arbitrary quantities, because the actual delay between the recorded signal and the time of the input step's transition is usually indeterminate. However, the portion of the phase spectrum that is not linearly related to frequency is often of interest, since this indicates effects on the phase due to the ADC under test. The *nonlinear phase* portion of the phase response can be made more apparent by unwrapping the phase (Souders et al. [B39]). A simple method to do this is to create a simple program to subtract 2π following each 2π discontinuity. Noise will usually impose a limit on how high in frequency such an approach can be effective. The result is a plot of the nonlinear phase contribution.

This test method makes use of the natural roll-off of the ADC under test as an anti-aliasing filter, attenuating the frequency components of the step that are beyond the Nyquist limit. Bounds on the magnitude and phase errors from aliasing and first differencing are given below, in 4.7.3.2.

Note that the digital differentiation operation accentuates high-frequency noise components, such as that due to quantization, and the equivalent noise increases as the square root of record length.

Ideally, $H(0)$ should equal the static gain as calculated in 4.3. This may not be the case, due to nonlinearities in the ADC, incomplete settling of the step signal, and other non-ideal behavior associated with the signal used for the test. Other non-ideal behavior could include: errors due to period-to-period jitter in the test square wave, i.e., short- versus long-term jitter effect on equivalent time measures; any hysteresis error introduced as the ADC cycles periodically through its saturated

and cutoff states; distortion due to bandwidth reduction architectures that translate harmonics by means of decimation filters; etc. These types of errors are all architecture dependent and so it is not possible to write general procedures to account for such effects.

4.7.3.2 Aliasing and first differencing error bounds

Bounds can be calculated for the errors in the dynamic gain or frequency response estimated above in 4.7.3.1. Assume that the frequency magnitude response of the ADC under test rolls off at least −20 dB per decade for frequencies higher than the −3 dB frequency (see 4.7.1), corresponding to the roll-off for a single pole. Then the aliasing and first differencing errors, $e_m[f]$, in the magnitude response, as measured above, will be no greater in magnitude (positive or negative) than (Souders et al. [B38]) as shown in Equation (123).

$$e_m(f) = \frac{400 \times f_{co} \times f}{f_s^2} \text{ \% of the step's amplitude at the ADC output} \quad (123)$$

$$\text{valid for } f < f_s/2 \text{ and } f_s \geq 2f_{co}$$

where

f is the frequency of interest,

f_{co} is the cutoff frequency (bandwidth (see 4.7.1)) of the test converter,

f_s is the sampling rate.

For the phase response, the aliasing and first differencing errors, $e_p[f]$, will be no greater in magnitude than (Souders et al. [B38]) as shown in Equation (124).

$$e_p[f] = 270\frac{f}{f_s} \text{ degrees} \quad (124)$$

$$\text{valid for } f \leq \frac{f_s}{4} \text{ and } f_s \geq 2f_{co}$$

EXAMPLE: If the expected cutoff frequency of the ADC under test is $f_{co} = 10$ MHz and an equivalent time sampling rate of $f_s = 100$ MHz is chosen, what is the maximum aliasing and first differencing error that can be expected at half the cutoff frequency (5 MHz)? [See Equation (125) and Equation (126).]

$$e_m = \frac{400 \times 5 \times 10^6 \times 10^7}{10^{16}} = 2\% \quad (125)$$

$$e_p = \frac{270 \times 5 \times 10^6}{10^8} = 13.5^\circ \quad (126)$$

As stated above, these error bounds assume that a single pole dominates the ADC's frequency response roll-off. Tighter error bounds may be applicable, in the case when the ADC's magnitude response rolls off at −40 dB per decade of frequency or faster, and when a correction is applied for the first-differencing error (Blair [B5]).

Note that these expressions give the upper and lower bounds only, and cannot be used as corrections.

4.7.3.3 Comment on frequency response tests

Significant amounts of nonlinearity and signal distortion in the ADC under test may result in inaccurate or even pathological values for frequency response, bandwidth, and gain flatness. Specifically, the errors in the step response caused by nonlinearity, as described in 4.6.1, can become errors in the measured bandwidth, gain flatness, and frequency response, as determined in 4.7.1, 4.7.2, and 4.7.3, respectively.

As noted in 4.6.1, the slew rate of the step signal used to determine the step response of the ADC has to be significantly below the slew rate limit, if any, in order to avoid nonlinearities.

4.8 Differential gain and phase

Differential gain and differential phase are parameters that quantify the suitability of circuits primarily for use with color composite video signals. These parameters are unrelated to any other gain or phase measurements outlined in this standard. They can and should only be measured on circuits specified to operate at bandwidths high enough to support the digitization of video test signals without aliasing.

In a National Television Standards Committee (NTSC) coded color video signal, the chrominance information is contained in amplitude-modulated 3.579545 MHz sub-carriers that are displaced in phase by $\pi/2$ radians. The luminance information, which can be used without color demodulation to decode the black and white portion of the signal, is broadcast as amplitude-modulated signal.

If the level of the luminance signal were to affect either the amplitude or the phase of the chrominance signal, then the resulting color displayed would not be the same as intended. Differential gain is present when the gain of the chrominance signal is affected by changes in the luminance level. Differential phase is present when the phase of the chrominance signal is affected by changes in the luminance level. Differential gain distortion causes incorrect color saturation; differential phase causes incorrect hues to be reproduced.

To test for differential gain and phase, a small amplitude sine of 3.58 MHz (or close to that) is measured for changes in sine-wave amplitude and phase as the dc offset is varied. Each dc offset represents a different value of amplitude-modulated luminance signal. As NTSC standards define differential gain as the largest amplitude deviation between any two levels, the number which should be reported is the worst-case peak-to-peak deviation of sine-wave amplitude over all luminance levels expressed as percent of the sine amplitude. Similarly, the number reported for differential phase should be the worst-case peak-to-peak deviation of sine-wave phase over all luminance levels, expressed in degrees. As a consequence of this definition, it is not necessary to specify differential gain or differential phase as signed numbers; the absolute value of the peak-to-peak error unambiguously meets the definition.

4.8.1 Method for testing a general purpose ADC

When testing a general purpose ADC (or any ADC that could be used with the sync tips at either end of the input range) it is important to scale and offset the input test signal so that almost all of the input full-scale range gets tested. In most applications this will involve setting a starting dc offset just large enough so that the 3.58 MHz sine-wave output code does not clip, and then increasing the dc offset until just before the sine-wave output code would begin to clip at the opposite peak.

The suggested test for a general purpose ADC uses a 6-level stepped waveform, generalized from National Television System Committee standard test signals of 140 IRE units peak-to-peak. While IRE units assume standard impedances and levels in volts, it is assumed here that an adjustable gain is placed ahead of the ADC under test in order to map the input full-scale range of the ADC to 140 IRE units. When this gain is adjusted such that the sine wave amplitude measures $40/140 = 28.6\%$ of the full-scale range peak-to-peak, then the gain from the sine source to the ADC is correctly mapped. When the dc steps change the output by $20/140 = 14.3\%$, then the gain from the stepped dc source is mapped correctly. It is further assumed that an adjustable offset has been summed with the input in order to keep the test signal from clipping at either end of the input range. The test setup is shown in Figure 13a and the waveform diagram is shown in Figure 13b.

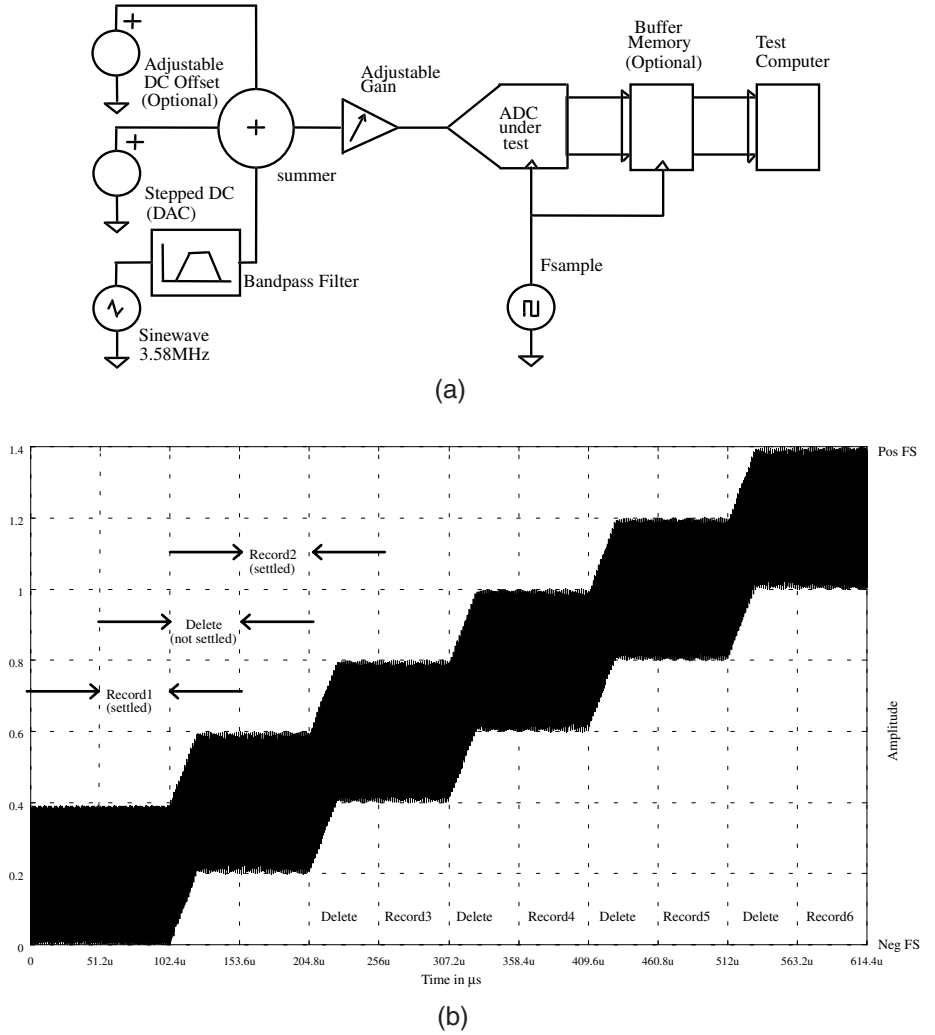

Figure 13—(a) Setup for differential phase/gain testing; (b) Example of stepped sinusoidal waveform used in differential phase and gain test

The waveform of Figure 13b uses six stepped dc levels of 20/140, 40/140, 60/140, 80/140, 100/140, and 120/140 of full scale at the ADC input. The test signal has been generalized from the NTSC standard test signal in that the length of time spent at each step has been made arbitrary, and the sync and timing information has been deleted.

In order to maximize the number of unique output codes obtained in each record, the input frequency and the sampling frequency should be picked such that the aperture point *walks through* the waveform. This requires that the sampling frequency NOT be equal to an integer multiple of the input sine frequency. Typically the sampling frequency is fixed at some value and the sine-wave input frequency is offset by a delta frequency sufficient to force at least one walk-through within M samples, where M is the length of each record sent to the FFT/DFT routine. If the input sine generator is only capable of generating exactly 3.579 545 MHz, then the ADC sampling frequency should be offset by a small delta of sufficient value to force the aperture point to walk through a complete cycle of the sine at least once in each record.

If a coherent FFT or DFT based test is assumed, then the usual non-integer restrictions on the ratio of sampling rate to input frequency which guarantee aperture point walkthrough will apply. The use of a

non-windowed FFT imposes an additional requirement that an integer number of cycles of the sine wave be present in the record length chosen. When combined, these conditions are equivalent to requiring the aperture point to walk through a complete integer number of cycles within each record. These considerations result in the following restrictions shown in Equation (127) (also see 4.1.4.3):

a) J and M are mutually prime.

b) $$f_i = \frac{f_s J}{M} \quad J = 1, 2, 3, \ldots \tag{127}$$

where

J is some integer to be chosen, usually less than $M/2$,

M is the number of samples in each record input to any FFT/DFT,

f_s is the ADC sampling frequency,

f_i is the frequency of the input sine.

If M is chosen to be some power of 2, such as 2048, then any J that is odd is mutually prime to M. In this case the odd number J yielding the frequency closest to 3.58 MHz could be chosen to get the input frequency. If the source to be used is constrained to 3.579 545 MHz, then the relation above should be solved for the appropriate f_s.

The suggested test of a general purpose ADC acquires one long contiguous record of ADC digital output data. Records 1 through 6, small pieces of the contiguous record, are each sent to an FFT, which yields complex data. The complex numbers corresponding to the frequency of the input sine wave are converted to magnitude/phase polar coordinates. One (usually the first) pair of magnitude/phase numbers is chosen to be the reference pair. The subsequent magnitude numbers from the FFT of records 2 through 6 are normalized to the reference magnitude and converted to percent change in magnitude.

The phase numbers are converted to degrees, and the reference phase is subtracted, yielding change in phase in degrees. In general, if the first phase is used as the reference, then the phase from subsequent FFTs must also be adjusted by subtracting the equivalent phase of the time delay between the beginning of the reference record and the record to be adjusted. This additional adjustment factor is computed as

t_d = delay in seconds between beginning of reference record and the beginning of the record being adjusted

where

Phase adjustment (degrees) is equal to $\mathrm{mod}_{360}\,(360 f_i t_d)$.

When the delay between records is set to exactly an integer number of record lengths, the above rules used to pick the input frequency will guarantee that the phase adjustment factor is zero (see 4.8.1.1). The phase adjustment factor may be useful in cases where the dc step settles in much less time than one record length, such as tests utilizing very long records. In this case the long continuous record will fit into a smaller memory size and some time which would have been spent waiting for the full record-length delay will be saved.

Five pairs of change in gain and change in phase numbers are obtained from the 6-level stepped waveform. If the amplitude change from the reference is positive for one change and negative for another, then the worst-case sum of the positive change plus the absolute value of the negative change

is reported as the differential gain. Similarly, if the change in phase is positive for one record and negative for another, then the worst-case sum of the positive change plus the absolute value of the negative change is reported. By convention, the reported numbers are always positive.

4.8.1.1 Method for neglecting phase adjustment factor

ADC output samples, which were acquired while the dc offset step was settling, are deleted. A smaller record of data beginning at some number-of-samples (delay = d) offset into the time record is kept. In order to guarantee that FFTs of an ideal ADC would show identically the same phase for each sub-record, it is necessary that records to be kept each begin with a sample of the sine wave at the same phase. If the frequency restrictions above have been followed, it is known that the input frequency will be at the same phase at each integer multiple of M samples. Thus the next record of data to be kept should begin at sample number = $d+lM$. The integer l should be chosen for each dc step to ensure that the small record to be kept occurs after the dc offset step has settled. In all, six small records of length M samples should be *kept* if a 6-level stepped modulated waveform is used as the test input. The waveform of Figure 13b shows the case where record length M is 1024 with $l = 2, 4, 6, \ldots$, and $d = 1024$ samples. It was assumed that f_s was 20 MHz and as shown in Equation (128).

$$f_i = \frac{183 f_s}{1024} = 3.57421875\,\text{MHz} \tag{128}$$

4.8.2 Method for testing a special purpose ADC

There may be systems which contain clamping or dc restoring circuitry or which require sync stripping for functionality or which for other reasons set the ADC input range such that the video information is never able to be found in portions at either end of the ADC input range. If the special purpose ADC or system is designed in this way, then a conventional NTSC test waveform should be used. The sine wave should start at a dc offset equal to the blanking level in its application (which could be at a dc offset of up to 23% of full scale). The dc offset should similarly be increased in steps toward the reference white level of the intended application, which will be at a level well before the sine-wave output code begins to clip. If the input full-scale range of the special purpose ADC is designed to allow user-adjusted gain before the ADC, then the full-scale input span should be mapped to 180 IRE units (as in a potential application which includes sync tips and a small amount of headroom within the input full-scale range). In this case a sine wave of $40/180 = 22.2\%$ of the full-scale range peak-to-peak corresponds to 40 IRE units.

Note that the gain and offset suggested above will never test sections of ADC output codes at the lower and upper end of its input range for their contribution to differential phase or gain errors. It is expected, due to the nature of the special purpose circuitry and its intended mode of operation, that these output codes will never be used in digitizing the active video portion of an NTSC signal.

If an NTSC standard signal generator is used, where the input frequency is constrained to be exactly 3.579545 MHz, the sampling frequency at the ADC should be adjusted as in 4.8.1 to ensure an integral number of cycles in the record length and thus produce spectral lines in the FFTs aligned with the center of their bin.

In the case where the sampling frequency is locked to a color burst which is derived from the input signal, a nonstandard input signal with an exact 3.579545 MHz color burst could be used, while the frequency digitized at each dc offset and used in the tests could be offset from this frequency. Systems where both the input sine frequency and the sampling frequency are constrained to an integer ratio may have to resort to extraordinary measures, such as repeated tests over multiple sine wave phases, or repeated tests using a ramped dc offset, in order to obtain the accuracy and repeatability available when testing over a wide alphabet of output codes.

Note that only two dc offsets are required to be tested during each horizontal interval; one sine at the reference dc offset and a second sine at the new dc offset. Thus, systems dependent upon sync information within an NTSC signal need not squeeze all dc offsets into a single horizontal interval as shown in standard waveforms. If dc offset settling times or FFT record length considerations warrant, the test can be spread over many sync intervals by acquiring records for only one pair of dc offset sinewaves in each horizontal interval.

4.8.3 Comments on differential phase and differential gain testing

The choice of generator(s) used for the tests can limit the achievable accuracy and resolution of the tests. While an arbitrary waveform generator could conceivably be used to provide the test stimulus of a combined stepped dc offset and sine wave, the DAC used in the generator and any filtering or de-glitching output circuitry present could color the measured results with its own differential gain and phase characteristics. A better solution uses a continuous low-phase-noise sine-wave source summed with a stepped dc offset. These signals may come from separate generators, each optimized in bandwidth for minimum noise.

The measurement of differential phase and gain for a phase alternation line (PAL) encoded video application can generally be regarded as an equivalent problem to the NTSC test except that the color sub-carrier frequency is defined to be 4.4332 MHz. This frequency should be used for the sine-wave test signal.

The method for testing general purpose ADCs utilizes an input waveform featuring user-chosen duration for each dc stepped sine segment. By making the length of each segment long, a record of 2048 samples or more may be used as the input to the FFT. The influence of quantization noise upon the results diminishes in proportion to the square root of the number of samples of each record. Using longer records enhances the repeatability of results.

The NTSC 40 IRE standard waveform contains offset sine waves from -20 IRE units to $+120$ IRE units, but also includes sync tips extending to -40 IRE. An NTSC waveform generator can be used to perform the general purpose ADC test by offsetting and scaling either the input signal or the ADC input range such that negative full-scale corresponds to -20 IRE and positive full-scale corresponds to $+120$ IRE.

When an NTSC standard test generator is used as the input source, the dc-stepped segments are of fixed duration. Typically only a short record length (≤ 64 samples) is possible for use in each FFT, and the repeatability of the results will be worse than if a longer record length were used.

Note that differential gain and phase are not the only error sources which affect the actual color of ideally reconstructed digitized NTSC video. Quantization noise is another major error source in the digitized video. When video is digitized on a well designed converter with a low number of bits, the quantization noise can exceed the color pollution effects of differential phase and differential gain by many times. The total instantaneous color pollution of a system will result from the sum of quantization noise degradations and the numbers measured here.

Other, earlier methods of testing utilized a reconstruction DAC and an instantaneous error display. The results displayed required visual interpretation to distinguish that portion of the instantaneous error due to quantization noise from that due to systematic differential phase or gain distortion. The tests of this standard, unlike earlier methods, yield measurements of differential phase and differential gain that are inherently distinct from the effects induced by quantization noise. Quantization noise will affect the repeatability of the numbers measured here, but this random variation can be made arbitrarily small by increasing the record length M.

A similar test method was used in Carbone [B6].

4.9 Aperture effects

To first order, an output value produced by an ADC represents a weighted average of the analog input signal over some period of time. The term *aperture* can refer to this period of time in general, or more specifically to the weighting as a function of time during this period. By the latter definition, the aperture, or aperture weighting function, is the time reversal of the impulse response of the ADC.

4.9.1 Aperture width

Aperture width is closely related to the transition duration of the step response. Unless otherwise indicated, aperture width is the full-width at half-maximum (FWHM) of the aperture weighting function. For a Gaussian aperture, this is roughly 0.92 times the 10% to 90% transition duration of the step response. Aperture width can also be described as the length of time necessary to encompass a specified percentage of the area under the aperture weighting function. The length of time necessary to encompass the center 80% of the area under the aperture is identically the 10% to 90% transition duration of the step response.

4.9.1.1 Test method

Record the step response of the ADC under test as described in 4.6. Take the discrete derivative of this record (see 4.7.1) to find the impulse response. Reverse the impulse response in time to find the aperture. The FWHM aperture width can then be determined by measuring the time from when the aperture first crosses above half of its maximum value until it last crosses below half its maximum value.

4.9.2 Aperture delay

Aperture delay is the delay from a threshold crossing of the ADC clock, which causes a sample of the analog input to be taken, to the center of the aperture for that sample. The center of the aperture is defined in Equation (129).

$$t_{wc} = \frac{\int_{-\infty}^{\infty} t \times w(t)\,dt}{\int_{-\infty}^{\infty} w(t)\,dt} \tag{129}$$

where

t is the time from the threshold crossing,

$w(t)$ is the aperture weighting function.

The aperture delay can be either positive or negative, depending on whether there is greater delay in the clock or the analog input path in the ADC.

4.9.2.1 Test method

Apply a ramp to the analog input and a clock to the clock input of the ADC. Instead of a ramp signal at the analog input, a portion of another waveform (e.g., a sine wave) can be used, provided that the slew rate of the waveform does not vary substantially over the aperture width of the ADC (e.g., a sine wave of frequency less than half the analog bandwidth of the ADC). The ramp signal slew rate should be as high as possible without exceeding the slew rate limit of the ADC's input or causing excessive dynamic errors. Synchronize the ramp and the clock such that the ADC samples the ramp at the center of the ADC's full-scale range. This can be done either by deriving both signals from the same frequency reference and adjusting the relative phase until the ADC's output values are at the center of its range, or by slightly offsetting the clock and ramp signal frequencies such that their relative phases will drift over time, and triggering the observation of the timing based on when the ADC's output values are at the center of its range. Using a

time-interval meter or oscilloscope of sufficient resolution and accuracy, measure the time delay from when the clock input crosses its threshold to when the analog input crosses the dc value corresponding to the center of the ADC's full-scale range. For ADCs with very high sample rate, where the aperture delay may be similar in magnitude to the clock period, extra care must be taken to ensure that the measurement is made from the correct clock edge. This can be done by repeating the measurement at various clock frequencies; the aperture delay as a function of clock periods should be roughly flat.

4.9.3 Aperture uncertainty

Aperture uncertainty, sometimes called *aperture jitter*, is the standard deviation of the aperture delay.

NOTE—The concept of aperture uncertainty can apply to ADCs that contain digital filtering of the output data (e.g., sigma-delta ADCs), even though the aperture for a given output value cannot be associated with a single clock edge, if a sufficiently stable clock source is applied to the ADC. An arbitrary decision can be made about which clock edge to associate with the sampling of a given output value, so long as the association is consistent across all samples taken during the measurement of the aperture uncertainty. Aperture uncertainty in a given setup may depend on the transition duration and noise on the clock signal (see 4.7.1).

4.9.3.1 Test method

Couple the output of a stable signal generator to both the analog input and the clock input of the ADC, using appropriate signal splitters, attenuators, dc blocks, frequency multipliers/dividers, etc., to ensure that the signal amplitude, offset, and frequency at each port are appropriate for that port. If at all possible, do not use any active components in this coupling, as any jitter in those components would contribute to the overall measured aperture uncertainty. The slew rate of the signal at the analog input port should be as high as possible without exceeding the slew rate limit of the ADC's input or incurring significant attenuation due to the bandwidth limitations of the ADC's input, as measured using the test methods of 4.7.1 or 4.7.2. An inadequate slew rate signal at the analog input port would result in inadequate aperture uncertainty measurement sensitivity, whereas an excessive slew rate signal would result in an estimate for the aperture uncertainty that is lower than the actual value. Adjust the delay of the path from the signal generator to the analog input port to be longer than the delay to the clock input port by the amount of the aperture delay (see 4.9.2), such that each active clock edge is sampling itself at its midpoint. If the frequency of the signal at the analog input is divided down from the clock frequency, decimate the output record by the same ratio and adjust the relative phase of the analog input and decimation dividers such that each recorded output value is a sample of the input signal at its midpoint. Measure the apparent random noise of the ADC in this configuration according to the test methods of 4.5.3. It may be necessary to add a summing node at the analog input port for low-noise ADCs in order to apply the slow triangle wave as well as the fast clock signal to the analog input. The apparent noise will include the effect of aperture uncertainty multiplied by the slew rate of the analog input signal. Break the connection between the signal generator and the analog's input port, and terminate both ends of the broken connection appropriately to prevent reflections. Measure the random noise of the ADC according to the test methods in 4.5.3. The aperture uncertainty is then given by Equation (130).

$$\sigma_T = \frac{\sqrt{\sigma_A^2 - \sigma_B^2}}{\text{slewrate}} \tag{130}$$

where σ_A^2 is the measured noise variance with a clock signal applied to the analog input port, σ_B^2 is the measured noise variance without the clock signal applied to the analog input port, and "slewrate" is the slew rate (magnitude of the slope) of the clock signal at the analog input port at the sampling instant.

4.10 Digital logic signals

Digital logic signals may be of many different types, depending on the ADC. The logic family name (TTL, ECL-100k, ECL-10k, etc.) should be used if the digital signals adhere to the standards for the family. If there are deviations from the standards (e.g., ECL outputs that must be terminated with odd value resistors due to insufficient current drive), then the differences should be clearly stated.

Users of ADCs will not usually need to measure the parameters of the logic signals, but manufacturers should do so to ensure compliance with accepted logic standards.

This section is worded in terms of a positive logic binary system, where the higher signal level (top) is associated with the binary value 1 and the lower (base) with the value 0. The changes to adapt to a negative logic system are straightforward. The determination of base and top can be accomplished using the histogram method, peak method, or user defined limits in accordance with IEC 60469-2 (1987-12) but the method used must be defined. The transition range is the range between the base and the top. In general, the logic parameters need to be determined under a suitable range of operating conditions. These include power supply voltages, input voltages, load impedances, and temperature.

4.11 Pipeline delay

Apply to the analog input a known steady-state signal different from that used to obtain the values currently on the output. Initiate a series of conversions. Use an oscilloscope and/or logic analyzer to observe the input, clock, and output signals. The pipeline delay is the number of clock cycles between the clock transition that initiates the conversion and the clock transition that causes the corresponding data to appear as valid data at the output. To prevent confusion between pipeline delay and aperture and/or propagation delays, the converter should be clocked at a low enough speed that the sampling of the analog input signal and the appearance of valid output data can each be unambiguously associated with a particular clock transition. The pipeline delay of an ADC is independent of the clock frequency. If the polarity of the clock transition at the start of conversion is the same as its polarity at the start of data validity, the delay will be an integral number of clock cycles. If the polarities are opposite, it will be a half-integral number of clock cycles. Note that even if the clock is asymmetric, each phase is considered to be one-half of a cycle.

4.12 Out-of-range recovery

An out-of-range input is any input whose magnitude is less than the maximum safe input value of the ADC but is greater than the full-scale value for the selected range. An out-of-range input may produce changes in the characteristics of the input channel, such as saturation of an amplifier or temporary changes in component values caused by thermal effects. The out-of-range recovery time is the time from the end of out-of-range to when the input channel returns to its specified characteristics. Out-of-range recovery occurs according to two different criteria. Relative recovery is achieved when the ADC's normal transfer characteristic is restored in all respects, except for signal propagation time through the ADC. Absolute recovery is achieved when the ADC's normal transfer characteristic is completely regained. Relative recovery is adequate when data before and after the out-of-range need not be related in time. When the data before and after the pulse must be related in time, then the ADC must recover absolutely.

4.12.1 Test method for absolute out-of-range recovery

Arrange a network capable of simultaneously applying both a high-purity sine wave and a specified out-of-range pulse (e.g., twice full scale) with a flat baseline. Apply a high-purity, large signal sine wave

of a convenient, non-harmonically related frequency (e.g., 1/20th the sampling frequency). Take a record of data with the out-of-range pulse occurring near the center of the record. Fit a sine wave to the data prior to the out-of-range pulse. Extrapolate the fitted sine wave to the end of the record. The measure of out-of-range recovery is the deviation of recorded data from the fitted sine wave. Out-of-range recovery time is measured from the last full-scale point associated with the pulse to the first point that deviates less than, and stays within, the desired tolerance of the fitted sine wave.

As a test of the method, record only the sine wave. Fit a sine wave to the portion of the record occurring prior to the point at which the out-of-range pulse will be introduced. Extend the fitted sine wave in the portion of the record where the out-of-range recovery is expected to occur. The observed deviation indicates the resolution obtainable when the pulse is applied.

4.12.2 Test method for relative out-of-range recovery

When the occurrence of events before the out-of-range pulse is not relevant to data acquired after the pulse, relative recovery is an appropriate criterion. Relative recovery may also be used when record length precludes the above method. To measure relative recovery, first record several records of the sine wave. Fit each record of data with a sine wave. Find the average amplitude, frequency, and dc offset of the fitted sine waves. Take a record of data in which the out-of-range pulse is removed very early in the record. Synchronize the previously fitted, average sine wave to the latter portion of the record (e.g., the last F record) by varying the phase only. Extend the synchronized sine wave across the entire record. Observe deviations as before.

4.12.3 Comments on test methods

In a high-frequency 50 Ω system, the sine wave and the pulse must be added using a resistive adder. An isolating reactive adder generally does not work because the top of the test pulse droops due to the adder's limited low-frequency response. This droop causes an undershoot when the pulse returns to its initial level. The resistive adder feeds some of the pulse back to the sine-wave generator, which may degrade the quality of the sine wave. This effect can be checked by performing the test on a sine wave/pulse combination that does not go beyond the full-scale of the ADC. Placing as large an attenuator as possible at the sine wave input to the resistive adder can reduce the degradation.

The out-of-range test pulse must return cleanly to its initial level. Any aberrations degrade the sine fit results.

4.13 Word error rate

The word error rate is the probability of receiving an erroneous code for an input, after correction is made for gain, offset, and linearity errors, and a specified allowance is made for noise. Other terms for word errors are *spurious codes*, *sparkle codes*, and *flyers*. Typical causes of word errors are metastability and timing jitter of comparators within the ADC.

4.13.1 Test methods

Since the word error rate is small (usually measured in parts per million or parts per billion), a great many samples must be collected to test for it. The number of samples required is discussed in Annex A. Before starting, choose a qualified error level. This qualified error level should be the smallest value that excludes all other sources of error from this test. Particular attention should be paid to excluding the tails of the noise distribution as a source of word errors. The sample rate must be specified with the test results.

4.13.1.1 Static test method

Because this test uses a slowly varying input signal, it is considered a static test. To test for word errors under high slew rate conditions, the dynamic test of 4.13.1.2 should be used.

Apply to the input of the ADC under test a large symmetric triangular signal whose amplitude range slightly exceeds the full-scale range, and whose rate of change is significantly less than the equivalent of 1 Q per sample period. Ensure that the peak-to-peak noise of the input signal does not exceed one least significant bit. Take the largest possible record of data. Examine the differences between successive samples, which are within the full-scale range of the ADC, and record the number of times this difference magnitude exceeds the qualified error level. A single word error will usually cause two successive large differences, one positive and the other negative. These two transitions count as one error. However, there can be special cases such as two successive word errors, or a transition which barely qualifies in one direction but not in the other, where there is only one transition per word error. Care should taken to count these correctly. Take successive records of data and keep a running total of qualified errors until the required number of samples has been examined.

The word error rate is the number of qualified errors found through the test method and divided by the number of samples examined.

4.13.1.2 Dynamic test method

This test uses a large amplitude, high frequency sine wave input signal to look for word errors in all code values, use the sine wave test setup (Figure 3). Apply to the input of the ADC under test a sine wave of known frequency whose amplitude is slightly larger than that needed to cover the full-scale range of the ADC. Because the input is a sine wave, the slew rate is different for each code value. Thus, this test uses a range of slew rates and the user needs to specify what the range is. The maximum slew rate occurs at mid-scale and the minimum slew rate occurs at the top and bottom of the full-scale range. These extreme slew rate values can be calculated as shown in Equation (131) and Equation (132).

$$\text{Slew}_{\max} = 2\pi f_{\text{i}} \times A \tag{131}$$

$$\text{Slew}_{\min} = 2\pi f_{\text{i}} \times A \times \sqrt{1 - 1/\rho^2} \tag{132}$$

where

f_{i} is the input sine wave frequency,

A is the sinewave amplitude,

ρ is the ratio of A to the amplitude that would give a full-scale signal.

The ratio ρ will have a value slightly larger than unity. By increasing ρ, the user can decrease the range of slew rates in the test, but care must be taken not to overdrive the ADC beyond the point where it works correctly. A ρ value of 1.15 is sufficient to reduce the ratio of $\text{Slew}_{\max}$ to $\text{Slew}_{\min}$ to 2.0.

Take a record of data and perform a sinefit to the data, using the sinefit routines of 4.1.4 but excluding data points that are off scale. Calculate the rms of the residuals of the data and then repeat the fit, this time also excluding data points with residuals more than the qualified error level, on the grounds that they are possible word errors.

The parameters of this second fit are used to construct the ideal values corresponding to the measured data. Compare the measured data to the ideal values and record the number of times the difference is greater than the qualified error level. Take additional data records until the required number of errors has been found (see 4.12.2) or the maximum number of samples has been taken.

The word error rate is the number of qualified errors found by the test, divided by the number of samples taken in portions of the data record not off scale.

4.13.1.3 Comment on the number of samples required for word error rate

While the formulation given in Annex A establishes the accuracy of the word error rate measurement as a function of samples taken, many users are not interested in knowing an exact word error rate, but are satisfied with an upper limit. To establish only that the error rate is less than some maximum, acquire at least ten times the number of samples for which it would be expected that a single word error would occur. For example, if the specification for the ADC application is that no more than one word error per million samples is allowable, acquire ten million samples. After acquiring and examining these samples, there are three possibilities as follows:

a) A few or no errors are found. Then the error rate is certainly less than the maximum.

b) The number of errors is approximately 10. A decision must be made now if the accuracy indicated by the equations in Annex A is satisfactory, or if it is necessary to acquire more data.

c) The number of errors is more than 10. If it is closer to 100, then the error rate is known with greater precision. In any case, the device under test exceeds the desired upper limit.

4.14 Differential input specifications

An ADC with differential inputs produces output codes that are a function of the difference between two input signals. The two input signals are typically called positive and negative. Such devices have a number of performance features in addition to those found in single-ended ADCs. These include the impedance of each input (positive and negative) to ground, maximum common-mode signal, maximum operating common-mode signal, common-mode rejection ratio, and common-mode out-of-range recovery time.

4.14.1 Input impedance to ground (for differential input ADCs)

This is the impedance between the positive input and ground or the negative input and ground. This impedance should be specified at several different frequencies. When the frequency is not specified, the impedance given is the static value. Alternatively, the input impedance can be represented as the parallel combination of a resistance and a capacitance.

4.14.1.1 Test method

Perform the measurement described in 4.2.1 or 4.2.2 for each of the inputs. When determining the impedance of the positive (negative) input, the negative (positive) input should be appropriately terminated and this termination should be specified.

4.14.2 Common-mode rejection ratio (CMRR) and maximum common-mode signal level

CMRR is the ratio of the input common-mode signal to the effect produced at the output of the ADC in units of the input, T_k. The output codes can be converted to input codes by using Equation (133).

$$V_{\text{out}} = Q[k-1] + T_1 \tag{133}$$

CMRR is normally specified as a Minimum value in dB. CMRR shall be specified at various frequencies. The maximum common-mode signal level is the maximum level of the common-mode signal at which the CMRR is still valid. The maximum common-mode signal level must also be specified.

4.14.2.1 Test method

Arrange a network capable of simultaneously applying identical amplitude sine wave signals to both differential inputs. The two common-mode signal levels must be identical to within the desired accuracy of the measurement. The common-mode signal level (V_{in}) must be large enough to discern an effect in the output data, and it must be equal to or below the specified maximum common-mode signal level. Take a record of data. Note the peak-to-peak level of the ADC output, V_{out}, converted into input units using Equation (135) at the common-mode sine wave frequency**.** Compute CMRR in decibels from [Equation (134)].

$$\text{CMRR} = 20 \log 10 \left(\frac{V_{in}}{V_{out}} \right) \tag{134}$$

If no common-mode signal is detectable in the output, assign V_{out} the value of $Q/2$. Repeat the measurement at common-mode frequencies of interest.

4.14.3 Maximum operating common-mode signal

The maximum operating common-mode signal is the largest common-mode signal for which the ADC will meet the effective number of bits specifications in recording a simultaneously applied normal mode signal.

4.14.3.1 Test method

Arrange a network capable of simultaneously applying identical-amplitude sine wave common-mode signals to both differential inputs and a normal mode large-signal sine wave test signal. Adjust the initial common-mode signal level to the specified maximum common-mode signal level. Take a record of data. Compute effective bits. Raise or lower the common-mode signal amplitude to determine the largest amplitude for which the effective bits specification is met. Repeat the measurement at common-mode and normal mode sine wave frequencies of interest.

4.14.4 Common-mode out-of-range recovery time

The common-mode out-of-range recovery time is time required for the ADC to return to its specified characteristics after the end of a common-mode out-of-range pulse. A common-mode out-of-range input is a signal level whose magnitude is less than the specified maximum safe common-mode signal but greater than the maximum operating common-mode signal.

Differential amplifiers often have poor CMRR at high frequencies and performance will be degraded following a high-level common-mode pulse. The output will typically be driven off scale by a common-mode pulse. Comments concerning absolute and relative recovery times for normal mode out-of-range inputs in 4.12 will in general apply for common-mode out-of-range inputs.

4.14.4.1 Test method for common-mode out-of-range recovery time

Arrange a network capable of simultaneously applying both a high-purity sine wave and a common-mode out-of-range pulse of specified amplitude, transition duration, and width. Measure absolute and relative recovery times as described in 4.12.1 and 4.12.2.

4.15 Comments on reference signals

Many ADCs provide for one or more reference signals, which can be either inputs to control or outputs to monitor operating characteristics. A common example is voltage references to set V_{min} and V_{max}, the minimum and maximum limits of the input signal. When specifying V_{min} and V_{max} it is necessary to state whether the mid-tread or mid-riser convention is being used.

When such reference signals are control inputs, it is necessary to understand the electrical properties, such as input impedance and capacitance. If there are dynamic aspects, such as a dependence of the impedance on the signal level or frequency, care must be taken to understand them.

If the reference signal is an output for monitoring, the drive characteristics must be well understood. Also, the accuracy and stability need to be determined, particularly under changes in environmental conditions, such as temperature.

Methods to determine the properties of reference signals are beyond the scope of this standard, in part because they may not be the same for all ADC architectures. It is important for manufacturers to specify them when appropriate and for users to understand their needs.

4.16 Power supply parameters

4.16.1 Power dissipation

Power dissipation refers to the average power dissipated by the device under test from the main power supplies to the device for a specific set of operating conditions. As the power dissipation may vary for different operating conditions, it is important that the setup used for determining the power dissipation be specified. The setup configuration should mimic actual operating conditions and include such things as clock signals and required output loads for proper operation.

Note that since power dissipation may vary depending upon several parameters (such as analog input voltage, clock polarity, etc.), it is mandatory to state the operating conditions for all inputs and outputs during this test. Manufacturers should try as many combinations as possible to arrive at the maximum dissipation configuration for the device.

4.16.1.1 Power dissipation test method

Connect the ADC under test to the appropriate power supplies set at specified, worst-case, or maximum, operating values for the device. Connect all appropriate signals necessary to operate the device as well as any necessary loads (i.e., signal termination resistors for inputs and outputs). Measure the current and voltage supplied to the device from each power supply. Compute the average power for each supply independently and sum these measures to determine the total power dissipation.

Annex A

(informative)

Comment on errors associated with word-error-rate measurement

There are statistical errors associated with word-error-rate measurements. Assuming the source of word errors is purely random and that both the number of observed word errors and the total number of trial samples are both statistically significant numbers (see 4.13.1.3), then the best estimate of error associated with the error rate, σ_e, is given as shown in Equation (A.1).

$$\sigma_e = \frac{[x(1-(x/S))]^{1/2}}{S} \tag{A.1}$$

where

x is the number of word errors detected,

S is the total number of trial samples,

For a given confidence level, $F[X]$, expressed as a fraction, the worst-case error rate w' is given by Equation (A.2).

$$w' = w + X\sigma_e \tag{A.2}$$

where

$w = x/S$ is the estimated word error rate (uncorrected).

X is the number of standard deviations covered by confidence $F[X]$ in a Gaussian distribution, and may be found in standard statistical tables.

A few examples of X and $F[X]$ (Table A.1) should cover most applications.

Table A.1—Gaussian distribution

F [X]	*X*
0.80	0.84
0.90	1.29
0.95	1.65
0.99	2.33

For some measurements, where word error rates are very low, x can be small or even zero. Equation (A.2) is an accurate estimate provided that x is not zero. For $x = 0$, one may calculate the probability, p, that not one word error would be seen for S trials, given an assumed worst-case error rate, w' as shown in Equation (A.3).

$$p = (1-w')^S \tag{A.3}$$

At a confidence level of $F[X]$, w' is bounded by the expression in Equation (A.4).

$$w' \leq 1 - (1-F[X])^{1/S} \tag{A.4}$$

For example, if $x = 0$ and $S = 100\,000$, using Equation (A.4), the worst-case word error rate is 3.0×10^{-5} or less with a 95% confidence level. For the same confidence level, using the σ_e from Equation (A.1) (and using the smallest non-zero value of x, $x = 1$) and solving Equation (A.2), a worst-case word error rate of 2.6×10^{-5} is determined. These results show consistency between Equation (A.2) and Equation (A.4).

Annex B

(informative)

Testing an ADC linearized with pseudorandom dither

B.1 Characteristics of ADC errors

The errors of an ADC are dependent upon its input signal. If the input signal is composed essentially of one (or two) frequency components, the ADC errors will typically be coherent with the input signal, and therefore most of the energy in the error spectrum will be harmonic or intermodulation distortion. The distortion can be particularly noticeable if the input signal amplitude is low; even an ideal quantizer can generate harmonic amplitudes comparable to the signal amplitude, if the input amplitude is on the order of the code bin width of the ADC.

One technique used to reduce such distortion is dithering, the combining of a dither signal with the input signal. A dither signal is a noise-like signal, often of wide bandwidth, intended to make the errors from ADC nonlinearities less correlated with one another. If the dither has a wide bandwidth, most of the energy in the error spectrum will be spread out into many frequency components, none of which will have large amplitude. The simplest dithering technique is to add low-level, wideband random noise to the ADC input signal (Gray and Stockham [B11]). However, just adding wideband random noise to the input signal can cause a significant reduction in the signal-to-noise ratio of the ADC, and may minimize harmonic distortion only for small-amplitude input signals. A dithering technique that is usually more effective for mitigating harmonic distortion is to add pseudorandom dither to the input signal, and digitally subtract an estimate of the dither from the ADC output. Pseudorandom dither is a waveform having the characteristics of random noise, but one that can be accurately repeated. Pseudorandom dither has been applied for television contrast (Roberts [B36]) and speech transmission applications. It is generated by repetitively cycling a digital-to-analog converter (DAC) or arbitrary waveform generator (AWG) through a sequence of values that generate a noise-like signal. It has been shown that when pseudorandom dither is added to a sinusoidal ADC input signal, the dither can randomize the ADC errors, so that they add incoherently and do not appear as significant harmonic distortion (Babu [B1]). For best results, the dither amplitude should be large, e.g., at least 25% of the ADC full-scale range, so that the errors from large-scale pattern errors can be averaged out. For some applications many ADC output measurements are averaged to improve the resolution. However, this does not work for converters whose internal noise is small compared to the quantization noise. A converter with a dither enables resolution enhancement by averaging.

A system in which the ADC is linearized with pseudorandom dither usually has two modes of operation. In the calibration mode, the input signal is switched off and the ADC measures only the pseudorandom dither and its effects. The dither is measured for many repetitions of its cycle, and the results are averaged, as described below, to provide an accurate estimate. In the normal mode of operation, the ADC measures the sum of the input signal and the dither. The estimate of the dither is digitally subtracted from the ADC output.

A test is presented in B.1.1, that shows how well the ADC will perform in a system which employs such pseudorandom dither linearization. If the test is designed correctly, with careful selection of the dither and the sine wave frequencies, a separate calibration mode is not needed in the test; only the normal mode of operation is required.

B.1.1 Pseudorandom dither test setup

The setup for pseudorandom dither testing is the same as that required for sine wave testing (see 4.1.1.1), except that an arbitrary waveform generator (AWG) replaces the lower-frequency synthesizer (sine wave generator). All the signal sources shall be synchronized by being phase locked to a master oscillator. There are three signal sources: the clock generator that triggers the ADC; the sine wave generator; and the AWG, which generates the pseudorandom dither signal. The input sine wave is filtered with a bandpass or lowpass filter to reduce its harmonic distortion, spurious distortion, and noise, and then combined in a resistive combiner with the dither signal. The digital output of the ADC is captured in data records.

Any suitable table or computer algorithm generates a random number sequence. The probability density function of the dither signal should be uniform because it is easier to generate, and allows a larger amplitude sine wave without clipping the ADC. This sequence may then be smoothed (digitally filtered) to reduce the noise bandwidth if desired, and then downloaded into the memory of the AWG. The AWG includes a digital memory, a precision DAC, and output amplifiers and filters. The digital codes controlling the DAC are temporarily stored in an internal digital memory in the AWG. The AWG repeatedly cycles through the waveform memory contents, generating a pseudorandom output waveform. The waveform repeats with a very high degree of stability because the AWG is phase locked to the master clock. The dither is adjusted for peak-to-peak amplitude of 10% to 45% of full scale of the ADC under test, and the sine wave input component is simultaneously adjusted, so that the combined signal amplitude nearly fills the full-scale range of the ADC under test.

For the recommended test, the sine wave and the pseudorandom dither are constrained to be orthogonal so that they can be separated digitally. For this test, the sine wave frequency and the dither repetition frequency are chosen so that there are exact integer numbers of periods of both the sine wave and repetitions of the dither waveform in the data record of length M samples taken by the ADC under test. Also, the numbers of periods of the sine wave and repetitions of the dither waveform should be relatively prime to one another. Note that this requires that the AWG must be set to clock at a frequency which is a rational fraction of the ADC clock, so that the AWG dither waveform has a repetition period which is an exact integer multiple of the ADC sample period.

Because there is an integer number of repetitions of the dither waveform in the data record, its spectrum will consist of only harmonics of the dither repetition frequency. The sine wave frequency is chosen to fall in between the harmonics of the dither repetition frequency, so that the dither is orthogonal to the sine wave. A computer program reads the record of data taken by the ADC under test, and calculates the Fourier components of the sine wave fundamental and its low-order harmonics. The pseudorandom waveform is estimated by averaging the data at corresponding points on the dither waveform, as described below. The sum of the fundamental sine wave estimate and the estimated dither is then subtracted from the recorded output. The difference is the estimated errors of the ADC; typically, their rms values and their spectrum are of interest.

The dither repetition period is chosen to be exactly equal to M_D ADC samples. Thus, M points in a data record represent J_D repetitions of the M_D -point pseudorandom waveform measurement vector, where $M = M_D J_D$. For each of the M_D points of the dither waveform there are J_D measurements of that dither voltage plus a sine wave. The phases of the sine wave at these J_D samples are uniformly distributed between 0 and 2π. To estimate the dither waveform, each sample in the output record is averaged with the other points that are integer multiples of M_D samples away from it in the record (i.e., with the other points in the data record that are at corresponding points in the repetition of the dither waveform). This generates a dither estimate record M_D samples long. Averaging J_D measurements in this manner, the sinewave component averages to 0, because there is an integer number of sinewave cycles in the data record.

Since the dither estimate is computed on the basis of an average of J_D points, the standard deviation due to random noise of each computed point is $(1/M_D)^{0.5}$ times the system noise level. The noise and errors of an ADC are typically on the order of 1 least significant bit (LSB), so the calculated estimate of the pseudorandom dither has less random noise, typically on the order of 0.1 LSB. The estimated dither and sine wave fundamental components are subtracted from the measured output to compute the estimated ADC errors. From the spectrum of the errors, it is possible to determine the parts of the errors due to the lower-order (e.g., 2nd through 10th) harmonic distortion, or the remainder due to higher-order harmonics and random noise.

B.1.2 Pseudorandom dither estimation

The output data record of the ADC under test is a series of M samples, V_n, for $n = 0,1,\ldots,(M-1)$. The input signal consists of the combination of the pseudorandom dither and a sine wave, which at the sampling instants have values d_n and f_n, respectively. If the ADC samples have small errors, $e[n]$, then [Equation (B.1)]

$$v[n] = d[n] + f[n] + e[n], \qquad \text{for } n = 0, 1, 2, \ldots, M-1 \tag{B.1}$$

The dither signal is phase locked to the sample clock, and repeats with a period of exactly M_D samples. Hence, it can be completely defined by the first M_D samples in the dither waveform measurement vector, f_i. There are exactly M_D cycles of the dither in the M samples, where $J_D = M/M_D$ [see Equation (B.2)].

$$d_u = d_i, \quad \text{where } u = (i\text{MOD } M_D), \qquad u = 0, 1, 2, \ldots, (M_D - 1) \tag{B.2}$$

The estimate of the repeated dither portion of the output signal, $d[m]$, for $m = 0, 1, 2, \ldots, (M_D-1)$, can be found by averaging the measurements made at the corresponding points of the data record as shown in Equation (B.3).

$$d_{est}[m] = \frac{1}{J_d}\sum_{k=0}^{J_d-1} v[m + kM_D], \qquad \text{for } m = 0, 1, 2, \ldots, (M_D - 1) \tag{B.3}$$

or, in other words [Equation (B.4)],

$$d_{est}[m] = d[m] + \frac{1}{J_d}\sum_{k=0}^{J_d-1} \varepsilon[m + kM_D], \qquad \text{for } m = 0, 1, 2, \ldots, (M_D - 1) \tag{B.4}$$

Note that, in the above equation, the error summation term is small because of the $(1/J_D)$ scale factor.

Example

Assume that we wish to test an ADC with a sine wave of approximately 12 MHz, using an ADC sample rate of $f_s = 25$ MHz. Also assume that the AWG sample frequency is $f_{AWG} = 10$ MHz, and that we load a sequence of 256 random numbers into the memory of the AWG. The output of the AWG changes every 0.1 μs, so the dither repeats with a period of 25.6 μs, or a frequency of 39.0625 kHz. If we wish the data record to contain $J_D = 100$ cycles of the dither, the data epoch must be 2560 μs long. At an ADC sample rate of 25 MHz, this corresponds to a data record length of $M = 64\,000$ samples. Typically, one might collect a record that is 64K = 65 536 samples long, and then discard the last 1536 samples. In the 25.6 μs dither repetition period, the ADC collects 640 samples, so M_D is 640. The sine wave frequency must be chosen to produce an exact integer number of cycles in the 2560 μs data epoch, i.e., a multiple of 390.625 Hz, which is the resolution of the 64 000-point DFT of the output record. A frequency of exactly 12 MHz is the 30 720th harmonic of 390.625 Hz, but is not suitable because the ADC would repeatedly sample only 25 points of the sinewave. For best results, we choose a prime number close to 30 720, such as 30 727, to multiply by 390.625 Hz, resulting in a sinewave frequency of 12 002 734.375 Hz.

The 640 points in the estimated dither vector are evaluated by

$$d_{\text{est}}[m] = \frac{1}{100}\sum_{k=0}^{99} v[m + 640k], \qquad \text{for } m = 0, 1, 2, \ldots, 639 \tag{B.5}$$

The sine wave parameters are found by evaluating the 30 727th term of the (64 000 point) DFT $V[k]$ of the data record $v[n]$, i.e., the $k = 30\,727$th Fourier coefficient, where $\omega = 2\pi \times 30\,727/64\,000$:

$$A_{\text{s}} = \frac{2}{64\,000}\sum_{n=0}^{63\,999} v[n]\sin(\omega n), \quad A_{\text{c}} = \frac{2}{64\,000}\sum_{n=0}^{63\,999} v[n]\cos(\omega n)$$

$$A = \sqrt{A_{\text{s}}^2 + A_{\text{c}}^2}, \quad \theta = \tan^{-1}\left(\frac{A_{\text{s}}}{A_{\text{c}}}\right)$$

$$\varepsilon_{\text{est}}[n] = v[n] - d_{\text{est}}[n \text{ MOD } 640] - A\cos(\omega n + \theta)$$

Annex C

(informative)

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